

## Article

# Modified SPWM Control for the Single-Stage Differential Boost Inverter Applying in Battery Energy Storage System

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**Abstract:** This study aims to implement a SSDBI (single-stage differential boost inverter, SSDBI) applying in a single-stage BESS (battery energy storage system, BESS) topology, which can supply power from lower voltage battery module to AC load. Compared with the common two-stage topology, which has a two-stage converter and higher voltage battery module array, the single-stage topology can reduce the number of cells and components, and improve the power density. In addition, a modified SPWM control was proposed to reduce the control complexity of the SSDBI while improving the THD of the inverter. The modified SPWM control can reduce the duty ratio of the SSDBI and the stress on the components to improve the AC voltage output waveform and reduce the THD value about 2.654%.

**Keywords:** boost inverter; modified SPWM; differential inverter

## 1. Introduction

Nowadays, the technology of inverters has been increasingly developed because there are numerous applications widely using inverters, such as PV and power grids. And the inverters and battery storage systems are one of the most popular combinations. The inverter plays an important role in the BESS, where the inverter is responsible for the energy transmission. Figure 1 shows the most familiar block diagram of the BESS, which includes a battery module array, a battery charger and an inverter[1]-[3]. First, AC Source (utility power) can charge the battery pack through the battery charger. Next, the inverter can extract the energy from battery pack to AC Load. At last, the battery pack will be responsible for the whole power supply when the AC Source is back out.

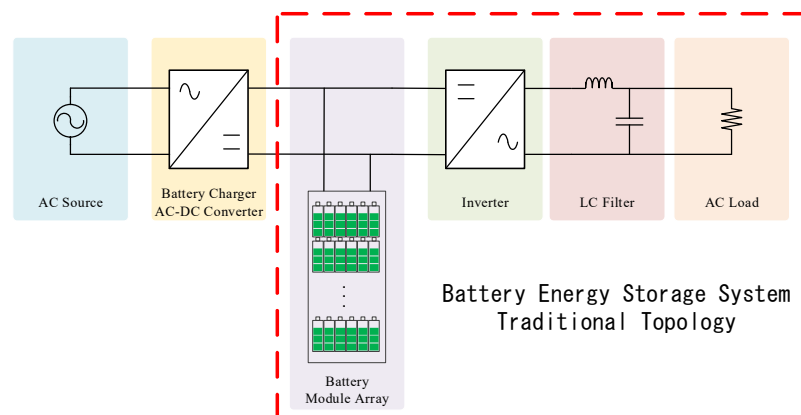


Figure 1. The block diagram of the BESS with a battery charger

However, it does not make economic sense using the BESS structure shown in Figure 1. The first reason is that a single cell's voltage is quite low. For example, the voltage of the lead-acid, the Ni-Cd, and the lithium-ion batteries are 2.0, 1.2, and 3.7 V, respectively. And the common BESS's needs high voltage, such as 380~400 V<sub>dc</sub>, for the inverter to supply power to the AC load. Under this condition, the battery module array should be composed of numerous cells connected in series. The high voltage battery module array will also lead to another problem, which is the cell SOC (state of charge, SOC) imbalance. If the imbalance problem comes out, some of the cells will be overcharged or over-discharged under the long-term work. Their SOH (state of health, SOH) will also decrease, even permanently damaged[4]-[6]. Furthermore, the BMS (battery management system, BMS) will be more difficult, more expensive and more dangerous when the battery module array's voltage becomes higher.

To overcome the aforementioned problem, the two-stage topology has been raised[7]-[8]. The structure included a battery module, a DC-DC converter, an inverter, DC bus capacitors and AC Load, as shown in Figure 2. The topology used a battery module with an additional DC-DC boost converter instead of a high voltage battery module array. However, large DC bus capacitors were a must for these topologies to connect the DC-DC converter with the inverter. Compared with the traditional topology, the two-stage topology is easy to implement and has a quite mature technology but the number of the components and their short lifetime and large size.

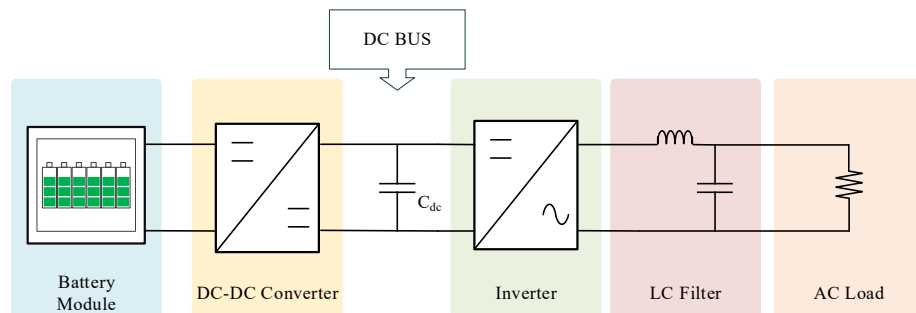


Figure 2. The traditional topology of the BESS

Figure 3 displays the Pseudo DC-link topology, which includes a low voltage battery module, DC-DC converter, inverter and AC load[9]-[10]. The difference between two-stage topology and Pseudo DC-link topology is the switch operation of the DC-DC converter. The switching control signal of the DC-DC converter in Pseudo DC-link topology is based on SPWM (sinusoidal pulse width modulation, SPWM) instead of traditional PWM (pulse width modulation, PWM). Therefore, in the Pseudo DC-link topology, the output of the DC-DC converter and the input of the inverter are the rectified sinusoidal waveform. The topology can convert the low voltage of the battery module to the rectified sinusoidal waveform with the DC-DC converter. And the voltage of the rectified sinusoidal waveform is high enough for the inverter supplying power to the AC load. The Pseudo DC-link topology can get over the need of the large capacitors in the traditional two-stage topology. And also, the operation efficiency of the inverter will increase because of the switching frequency reduction. Nevertheless, the Pseudo DC-link topology is still a two-stage topology with plenty of the components the same as the traditional two-stage topology.

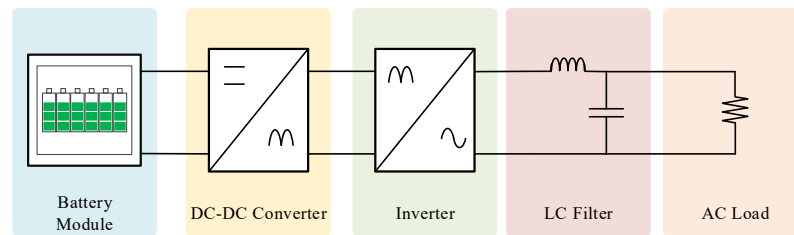


Figure 3. Pseudo DC-link topology of the BESS

For further improvement, the single-stage topology was proposed by recent research to minimize the used components[11]-[12]. Figure 4 shows the single-stage topology including a battery module, a single-stage inverter and AC load. The single-stage inverter has a good performance in adjusting the voltage and gives an AC output instead of a DC-DC converter and inverter combination. Compared with the two-stage topology, the single-stage inverter in the single-stage topology is not mature enough and too complicated to implement.

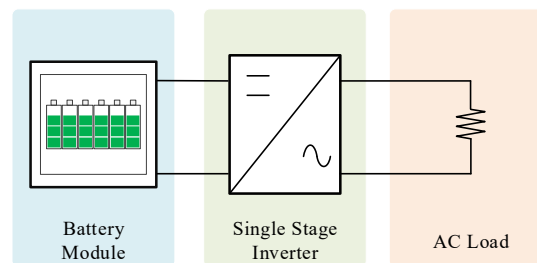


Figure 4. The single-stage topology of the BESS

This study proposed a single-stage inverter, as displayed in Figure 5, which is also called a SSDBI (single-stage differential boost inverter, SSDBI). Compared with others[11]-[12], the purpose of the proposed inverter is to provide energy from a low voltage battery module to a 110  $V_{ac}$  AC load but connect with the grid. The inverter has fewer components, which only consisted of two inductors, two capacitors, and four switches. Due to the characteristic of the structure, the converter uses high-frequency inductors instead of filter inductors to reduce the cost and the size of the inductor. And the capacitors are not used to store an amount of energy, so the capacitance and the size of the capacitors become more low-cost and smaller.

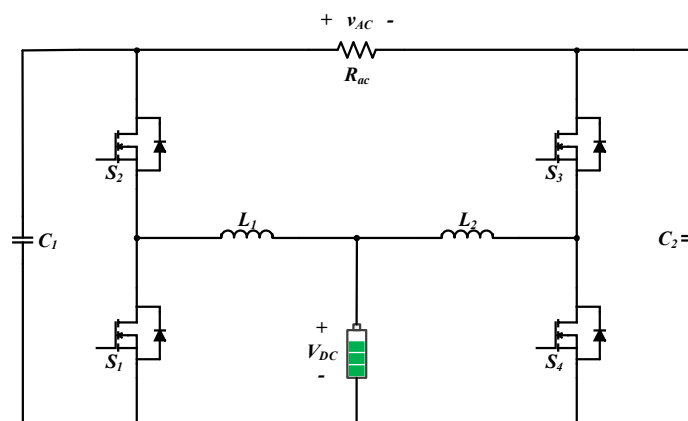


Figure 5. The schematic of the SSDBI

In the previous studies, researchers raised the controls based on the proposed single-stage inverter[13]-[17]. Damith B. Wickramasinghe Abeywardana and Woei-Luen Chen respectively proposed a control combining PI control (proportional integral control, PI control) with PR control (proportional resonant control, PR control). The control compensated the capacitor's voltage with PR control and then the inductor's current with PI control. This control had better AC voltage stability while adjusting and limit the inductor's current. However, the control was a double loop compensator, which was difficult to stabilize both the outer-loop and the inner-loop[13]-[14]. Diana Lopez-Caiza and Oswaldo López-Santos raised SMC (sliding mode control, SMC), separately. Through the discontinuous control, the SMC would keep adjusting the inductor's current and the capacitor's voltage until the inverter worked in stable condition. The SMC was suitable for the SSDBI because it could control the non-linear current and voltage individually. The SMC could also reduce the THD of the inverter, but the SMC needs plenty of feedback signals and the design was also complicated. Kapil Jha used SPWM control, which simplified the design of the control at the cost of THD.

In view of the above research, this study modified the SPWM directed to the SSDBI. Through the steady-state circuit analysis, the simulations and the hardware experiments, the study verified the proposed inverter's feasibility and the control's modification, which considered the system's complication, cost and THD.

## 2. System description of SSDBI

This section describes the steady-state analysis of the SSDBI and the design consideration of the components.

### 2.1. Steady-state analysis of the SSDBI

For simplifying the analysis, the inverter can be separated into two parts, Converter 1 and Converter 2, because the inverter is a differential architecture. As shown in Figure 6, the direction and the symbol of the loops' current and voltage are defined and labeled, where  $V_{DC}$  and  $i_{DC}$  are the voltage and the current of the DC bus,  $v_{AC}$  and  $i_{AC}$  are the voltage and the current of the AC load,  $v_{L1}$  and  $i_{L1}$  are the voltage and the current of the inductor  $L_1$ ,  $v_{L2}$  and  $i_{L2}$  are the voltage and the current of the inductor  $L_2$ ,  $v_{C1}$  and  $i_{C1}$  are the voltage and the current of the capacitor  $C_1$ ,  $v_{C2}$  and  $i_{C2}$  are the voltage and the current of the capacitor  $C_2$ . According to Kirchhoff's Voltage and Current Law,  $i_{DC}$  is equal to the sum of the  $i_{L1}$  and  $i_{L2}$ ,  $v_{AC}$  is equal to the difference of the  $v_{C1}$  and  $v_{C2}$ .

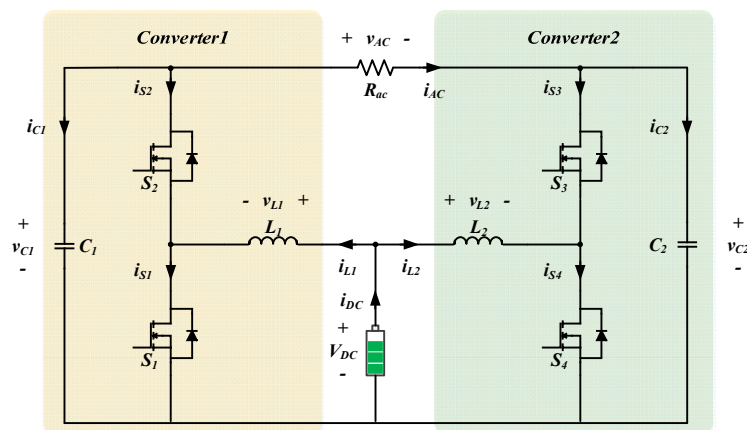


Figure 6. the analysis model of the SSDBI

Since the switching frequency of the inverter is much higher than the AC load's requirement, the inverter will perform multiple charging and discharging cycles with the

switching frequency in a period of the AC load. Therefore, the following will be introduced with a positive half period and a negative half period, respectively. Table 1 shows the operation mode of Converter 1 and Converter 2, and Figure 7 displays the operation states of the inverter. In the positive half period ( $v_{AC} > 0$ ), Converter 1 works as boost converter charging  $C_1$  with  $V_{DC}$  and Converter 2 works as buck converter charging  $V_{DC}$ . In the negative half period ( $v_{AC} < 0$ ), Converter 1 works as buck converter charging  $V_{DC}$  and Converter 2 works as boost converter charging  $C_2$ . Both Converter 1 and Converter 2 have similar operation modes in the positive (Mode 1 & Mode 2) and negative (Mode 3 & Mode 4) half periods. So the steady-state analysis will take the positive half period as an example.

**Table 1.** The operation mode of Converter 1 and Converter 2

$v_{AC}$	Mode	Status of switch	Status of converter
$> 0$	Mode 1	$S_1$ 、 $S_3$ on	Converter 1: Boost ( $V_{DC}$ Charges $C_1$ ) Converter 2: Buck ( $C_2$ Charges $V_{DC}$ )
	$[t_0 \sim t_1]$	$S_2$ 、 $S_4$ off	
	Mode 2	$S_2$ 、 $S_4$ on	
$< 0$	$[t_1 \sim t_2]$	$S_1$ 、 $S_3$ off	Converter 1: Buck ( $C_1$ Charges $V_{DC}$ ) Converter 2: Boost ( $V_{DC}$ Charges $C_2$ )
	Mode 3	$S_2$ 、 $S_4$ on	
	$[t_2 \sim t_3]$	$S_1$ 、 $S_3$ off	
$< 0$	Mode 4	$S_1$ 、 $S_3$ on	Converter 1: Buck ( $C_1$ Charges $V_{DC}$ ) Converter 2: Boost ( $V_{DC}$ Charges $C_2$ )
	$[t_3 \sim t_4]$	$S_2$ 、 $S_4$ off	

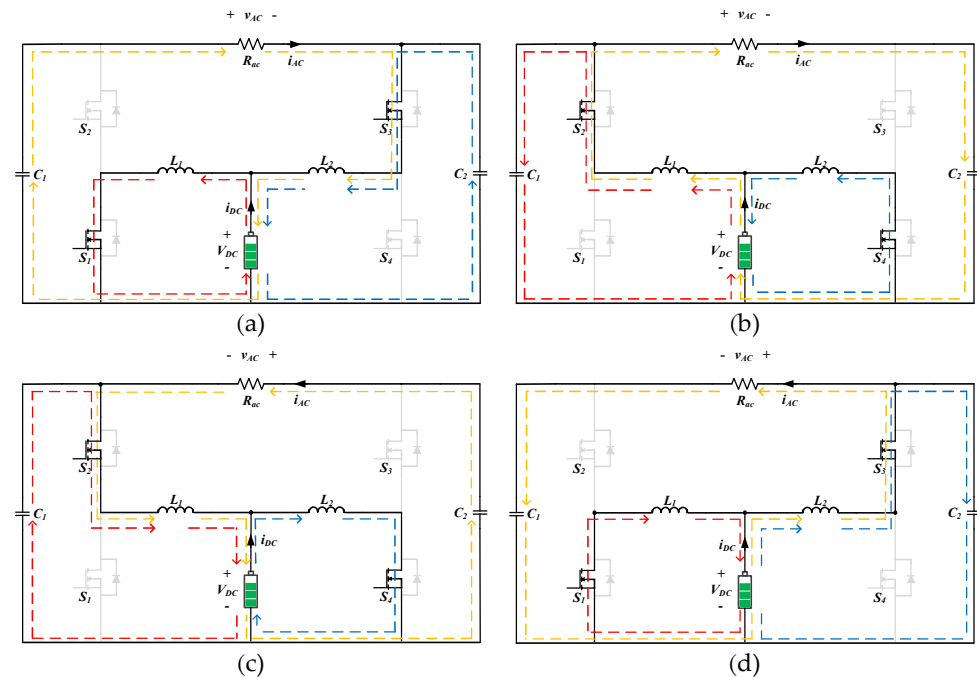


Figure 7. The operation states of the inverter (a)Mode 1; (b)Mode 2; (c)Mode 3; (d)Mode 4

Mode 1  $[t_0 \sim t_1]$ :

In Mode 1,  $v_{AC} > 0$ ,  $i_{AC} > 0$ .  $S_1$  on,  $S_2$  off,  $S_3$  on, and  $S_4$  off.  $L_1$ ,  $L_2$  are being charged and  $C_1$ ,  $C_2$  are discharging. The voltage across  $L_1$  is  $V_{DC}$ , the voltage across  $L_2$  is  $-(v_{C2} - V_{DC})$ . The current passed by  $C_1$  is  $-i_{AC}$ , and  $C_2$  is  $i_{L2} + i_{AC}$ . The variations of each inductors' current and capacitors' voltage can be obtained as follows:

$$\frac{di_{L1}}{dt} = \frac{V_{DC}}{L_1} \quad (1)$$

$$\frac{di_{L2}}{dt} = -\frac{v_{C2} - V_{DC}}{L_2} \quad (2)$$

$$\frac{dv_{C1}}{dt} = -\frac{i_{AC}}{C_1} \quad (3)$$

$$\frac{dv_{C2}}{dt} = \frac{i_{L2} + i_{AC}}{C_2} \quad (4)$$

Mode 2 [ $t_1 \sim t_2$ ]:

In Mode 2,  $v_{AC} > 0$ ,  $i_{AC} > 0$ .  $S_1$  off,  $S_2$  on,  $S_3$  off, and  $S_4$  on.  $L_1, L_2$  are discharging, and  $C_1, C_2$  are being charged. The voltage across  $L_1$  becomes  $V_{DC} - v_{C1}$ , the voltage across  $L_2$  becomes  $V_{DC}$ . The current passed by  $C_1$  changes to  $i_{L1} - i_{AC}$ , and  $C_2$  changes to  $i_{AC}$ . The variations of each inductors' current and capacitors' voltage are shown as following:

$$\frac{di_{L1}}{dt} = \frac{V_{DC} - v_{C1}}{L_1} \quad (5)$$

$$\frac{di_{L2}}{dt} = \frac{V_{DC}}{L_2} \quad (6)$$

$$\frac{dv_{C1}}{dt} = \frac{i_{L1} - i_{AC}}{C_1} \quad (7)$$

$$\frac{dv_{C2}}{dt} = \frac{i_{AC}}{C_2} \quad (8)$$

Through the aforementioned analysis, the equation (9) and (10) can be obtained by referring to (1), (2), (5), (6) and volt-second balance theory.

$$v_{C1} = \frac{V_{DC}}{1 - D} \quad (9)$$

$$v_{C2} = \frac{V_{DC}}{D} \quad (10)$$

We have already known that  $v_{AC}$  is equal to the voltage difference between  $v_{C1}$  and  $v_{C2}$ . Hence, the relationship between  $V_{DC}$  and  $v_{AC}$  can be calculated in (11).

$$v_{AC} = \frac{V_{DC}}{1 - D} - \frac{V_{DC}}{D} \quad (11)$$

After rearranging (11), the duty ratio  $D$  is expressed as below:

$$D = \frac{v_{AC} - 2V_{DC} + \sqrt{v_{AC}^2 + 4V_{DC}^2}}{2v_{AC}} \quad (12)$$

The gain of the inverter  $M$  is the ratio of  $V_{DC}$  and  $v_{AC}$ . Rearranging (12) once more,  $M$  and the relationship between  $M$  and  $D$  can be shown by the following.

$$M = \frac{2D - 1}{(1 - D)D} \quad (13)$$

$$D = \frac{M - 2 + \sqrt{M^2 + 4}}{M} \quad (14)$$

## 2.2. Design Consideration of the components

Through the analysis, it can be informed that the formula of Converter 1 in the positive half period is the same as the formula of Converter 2 in the negative half period. So, the capacitance of  $C_1$  and  $C_2$  are the same. Therefore, (3) can infer the design formula of  $C_1$  and  $C_2$ , as shown in (15), where  $\Delta v_{C1}$  is the ripple of the capacitor's voltage.

$$C = i_{AC} \frac{DT_s}{\Delta v_{C1} V_{C1}} \quad (15)$$

In addition, the design consideration of the inductors is similar to the capacitor. The formula of the design consideration can be inferred by (1), as shown in (16), where  $\Delta i_{L1}$  is the ripple of the inductor's current.

$$L = V_{DC} \frac{DT_s}{\Delta i_{L1} I_{L1max}} \quad (16)$$

## 3. The analysis of the control

### 3.1. The problem of traditional SPWM control applying to the proposed inverter

As known to all, there have already lots of control proposed for the inverter, where SPWM is the most mature one, the control is usually applied for buck inverters. Figure 8 shows the traditional SPWM control principle applying to the buck inverter, where the duty ratio  $D_{spwm}$  is generated by the comparison between a sine wave signal  $V_{control}$  and a triangular wave signal  $V_{tri}$ , the amplitude and frequency of  $V_{tri}$  are  $\hat{V}_{tri}$  and  $f_s$ ,  $\hat{V}_{control}$  represent the amplitude of  $V_{control}$ , and The sine wave's frequency  $f_i$  is the same as the output voltage frequency  $f$ [18].

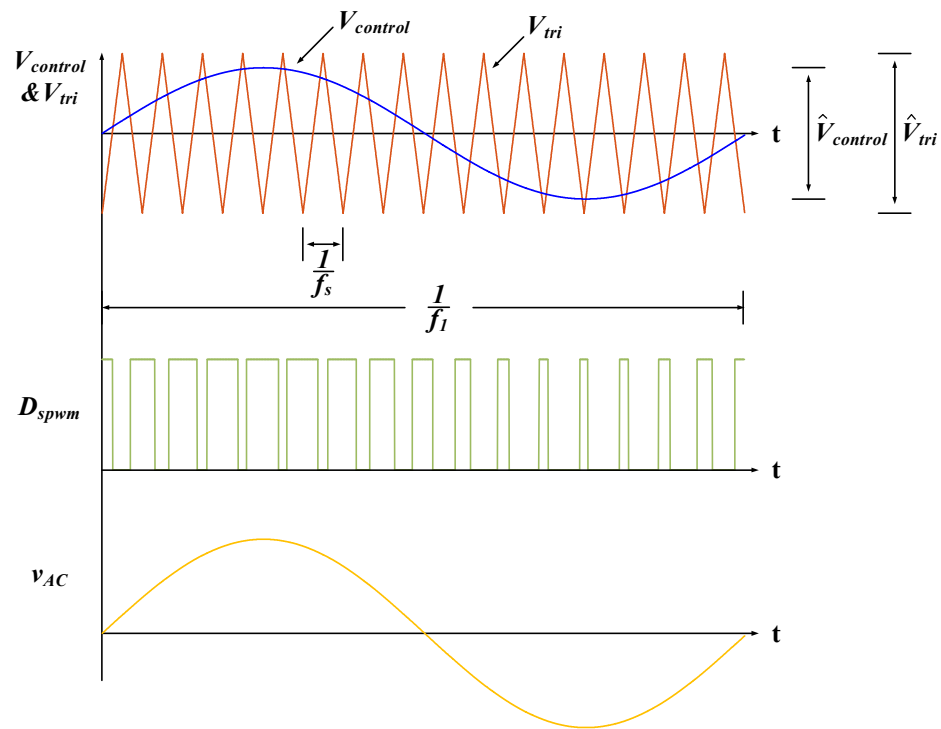


Figure 8. The relationship among the control signal, duty ratio and AC output  $v_{AC}$  in buck inverters with traditional SPWM control

The amplitude modulation index  $m_a$  is the ratio of  $\hat{V}_{control}$  and  $\hat{V}_{tri}$ .  $m_a$  can decide  $D_{spwm}$ , as shown in (17).

$$D_{spwm}(t) = \frac{1}{2} + \frac{V_{control}(t)}{2} = \frac{1}{2} + \frac{m_a \sin \omega t}{2} \quad (17)$$

Since SPWM is mainly used in buck inverters, the gain  $M$  must be less than 1, which is half of  $m_a$ . The formulas of  $M$  and rearranged  $D_{spwm}$  are shown in (18), (19).

$$M = \frac{v_{AC}}{V_{DC}} = \frac{1}{2} m_a = \frac{1}{2} \frac{\hat{V}_{control}}{\hat{V}_{tri}} \quad (18)$$

$$D_{spwm}(t) = \frac{1}{2} + \frac{V_{control}(t)}{2} = \frac{1}{2} + \frac{m_a \sin \omega t}{2} = \frac{1}{2} + M \sin \omega t = \frac{1}{2} + \frac{v_{AC}(t)}{V_{DC}} \quad (19)$$

If the DC voltage is assumed as a stable power supply, its value will be constant. Through the aforementioned formula,  $D_{spwm}$ ,  $v_{AC}$  and  $M$  will increase while  $V_{control}(t)$  increases. So,  $\hat{V}_{control}$  can be regarded as  $v_{AC}(t)$  with equally scaled reduced amplitude.  $M$  has a linear relationship with  $D_{spwm}$ .

However, if the mentioned above SPWM control directly uses in the SSDBI[17], the voltage of AC output will be distorted. As shown in Figure 9, the expected sine waveform of the AC output will become a waveform, which is similar to a triangular waveform.

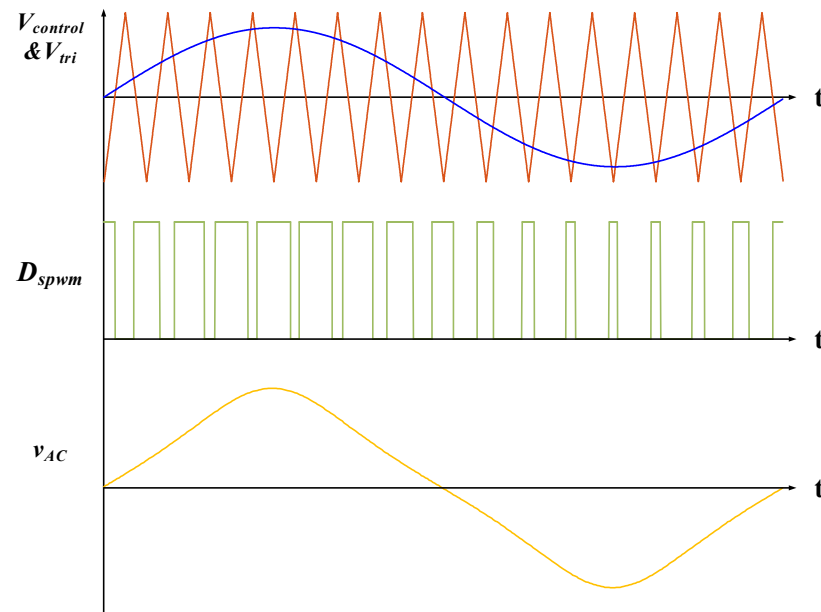


Figure 9.  $v_{AC}$  waveform generated by the proposed inverter with SPWM control

The reason for the distortion is that  $V_{control}$  still has the same relationship with  $v_{AC}$ ,  $D_{spwm}$  and  $V_{control}$ . But, the formulas among those parameters, as shown in (12), (14), are different from the buck inverter.

### 3.2. The proposed modified SPWM control

To overcome the distortion, this study proposed a modified SPWM control for the SSDBI. The proposed SPWM modifies a new formula for the new duty ratio  $D_{modified\_spwm}$ .

$$D_{modified\_spwm}(t) = \frac{v_{AC}(t) - 2V_{DC} + \sqrt{v_{AC}^2(t) + 4V_{DC}^2}}{2v_{AC}(t)} \quad (20)$$

We can get the modified  $V_{control}(t)$  by putting (20) into (17), as shown in (21). Although  $V_{control}$  has a new relationship with  $v_{AC}$ , the inverter driven with the  $D_{modified\_spwm}$  will have the expected sine voltage waveform of the AC output.

$$V_{control}(t) = 2D_{modified\_spwm}(t) - 1 \quad (21)$$

Figure 10 displays the comparison between traditional SPWM control and the modified SPWM control. In Figure 10(a), the comparison is focused on  $V_{control}$ , where the dotted line and the solid line represent  $V_{control}$  in the traditional SPWM control and the modified SPWM control, respectively. Figure 10(b) shows the voltage waveform's difference in the AC output. Through Figure 10, even if the traditional SPWM control gives a sine wave signal for the  $V_{control}$  in the proposed inverter,  $v_{AC}$  will be distorted. By contrast, the proposed SPWM control will have an expected sine voltage output with the modified  $V_{control}$ .

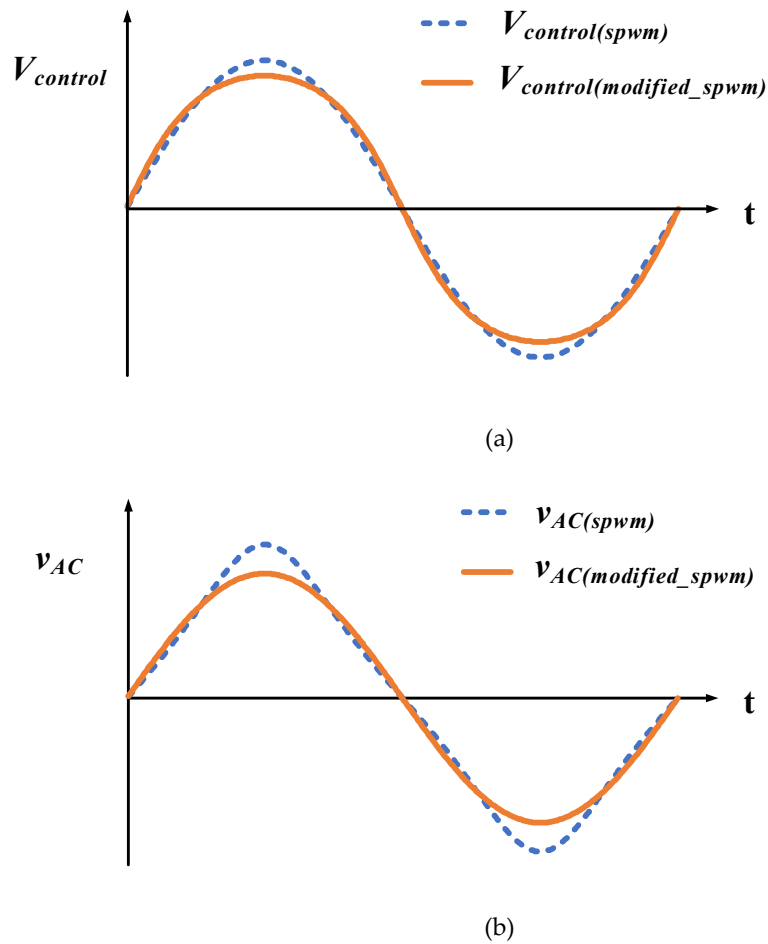


Figure 10. The comparison between traditional SPWM control and the modified SPWM control (a)  $V_{control}$  (b)  $v_{AC}$

4. Experiment results

4.1. System specification description

Figure 11 shows the experiment platform of the SSDBI, where the actual system configuration is displayed in Figure 12. In this study, the DC input is a 16S3P battery module, where a single cell (PC40155) is manufactured by PHOENIX BATTERY CORPORATION, the voltage range of the battery module is 33.6~58.4  $V_{dc}$ . The other system specification can also be obtained in Table 2.

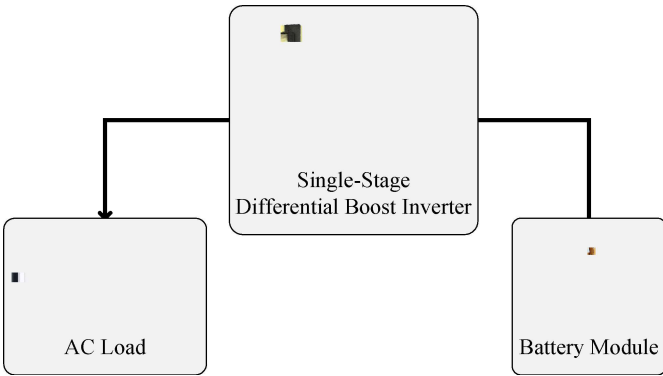


Figure 11. System connection of the SSDBI

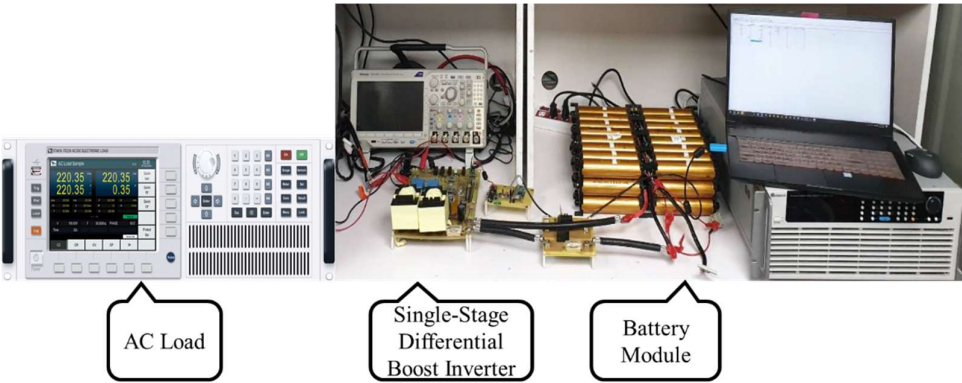


Figure 12. The laboratory setup of the test platform

Table 2. Specification of the proposed BESS

Item	Value
Battery module (voltage range)	33.6~58.4 $V_{dc}$
Battery module (voltage rated)	52.8 $V_{dc}$
AC output voltage	110 $V_{rms}$
Power	1000 W
Switching frequency	21.6 kHz
Inductor	120 $\mu H$ 、 120 $\mu H$
Capacitor	12 $\mu F$ 、 12 $\mu F$

4.2. Simulation and hardware experiment results

In this section, the proposed modified control is compared with the traditional SPWM with simulation and hardware experiment results. The simulation software Matlab used in this research is manufactured by MathWorks, Inc. (Natick, Massachusetts, USA).

First, this study compared the controls’ influence on the output waveforms with simulation, as shown in Figure13, where the traditional SPWM control was represented by dotted line, the modified SPWM control was displayed by solid line, the X-axis was for the time, and Y-axis was the amplitude of the  $V_{control}$ . From Figure 13, it can be obtained that  $V_{control}$  of the modified SPWM is not a sine waveform.

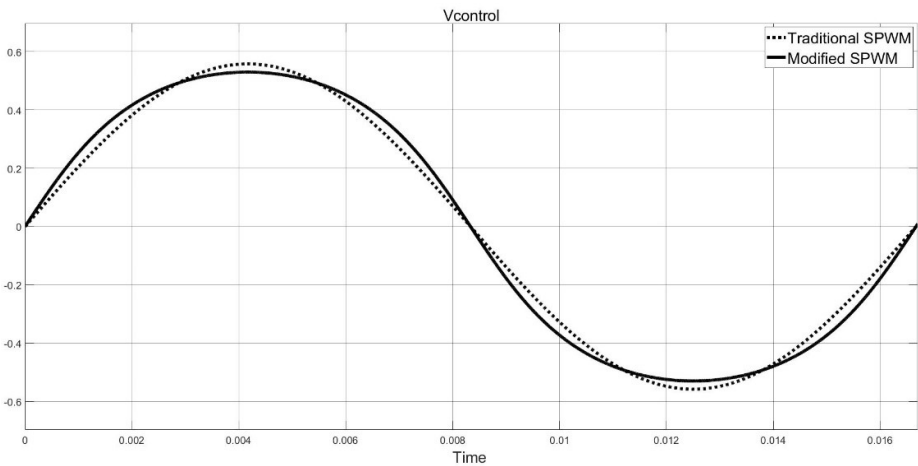


Figure 13.  $V_{control}$  comparison between traditional SPWM and modified SPWM controls

Secondly,  $V_{control}$  of both controls applied to the control loop to drive SSDBI in simulation, as shown in Figure 14. And the output waveform is displayed in Figure 15, where Figure 15(a) and Figure 15(b) show the voltage and current waveform with the traditional SPWM control and the modified SPWM control, respectively. Through analyzing the differences, it can be easily acquired that the proposed inverter applying the modified SPWM control has a better output in simulation.

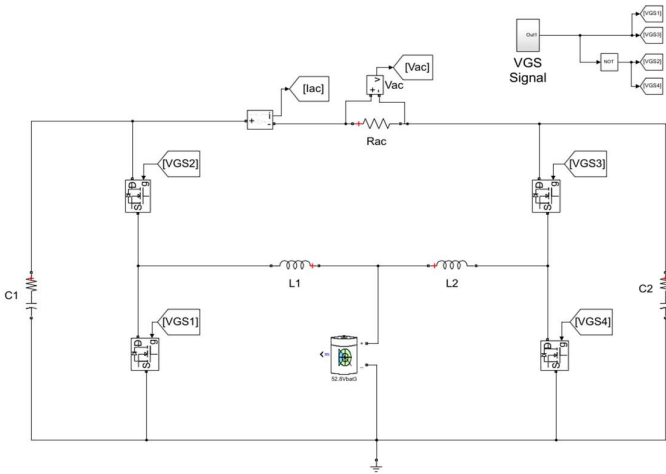
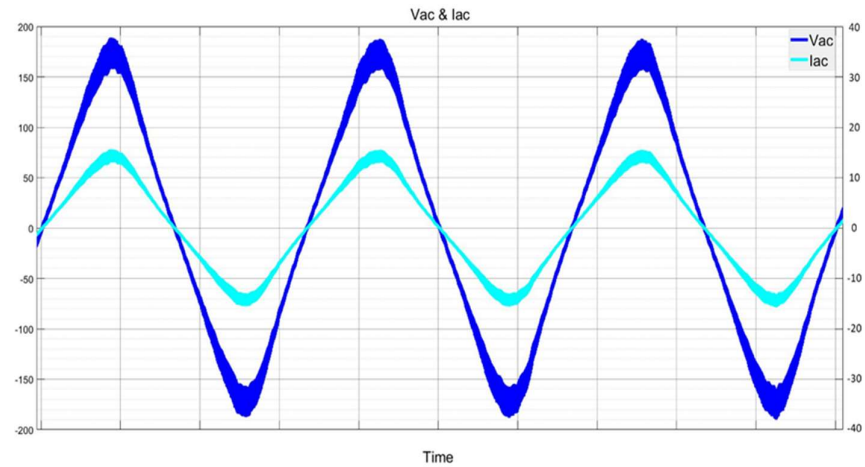
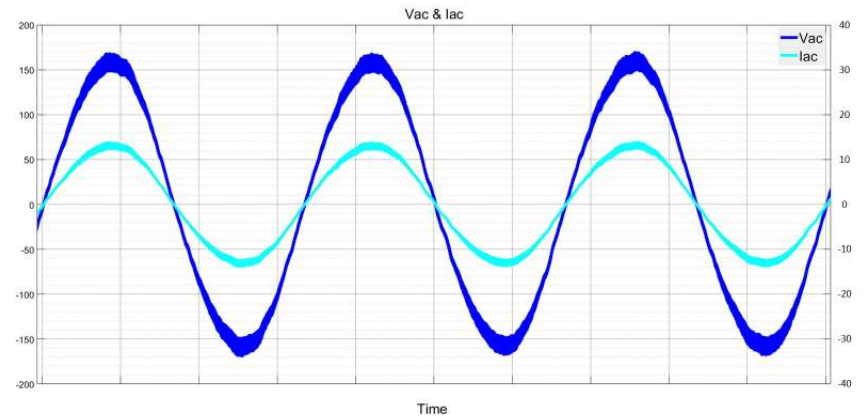


Figure 14. The circuit diagram of the implemented SSDBI in the simulation



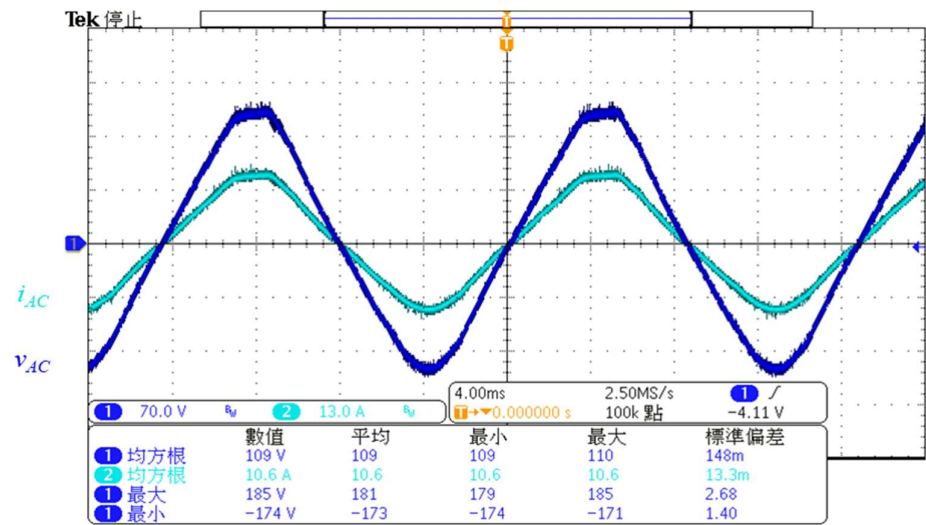
(a)



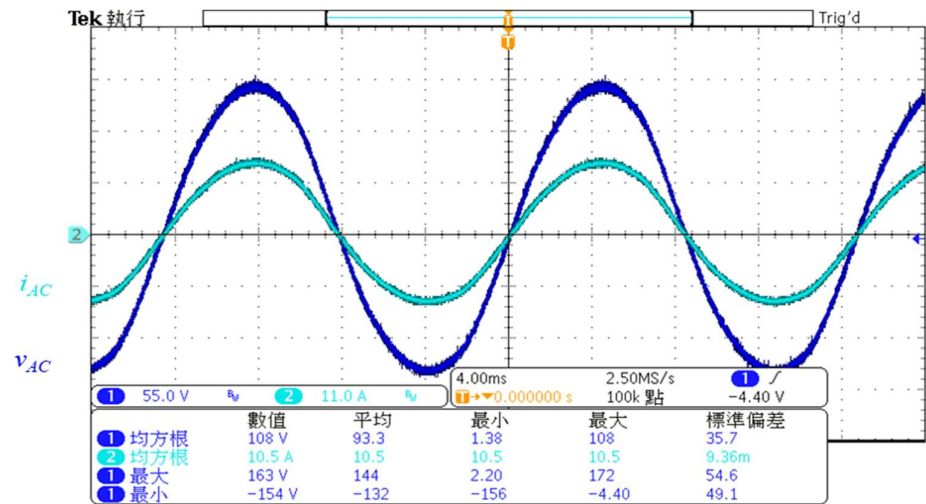
(b)

Figure 15. The simulation results of the voltage and current output waveforms using (a) traditional SPWM control; (b) modified SPWM control

For further verification, this study tested the SPWM controls by hardware experiments. The hardware experiment waveforms are shown in Figure 16. In Figure 16(a), (b), the results show that the traditional SPWM control needs a larger peak value of both the voltage and current than the modified one while reaching the same RMS(root mean square, RMS). This problem will lead to the increment of the system specification.



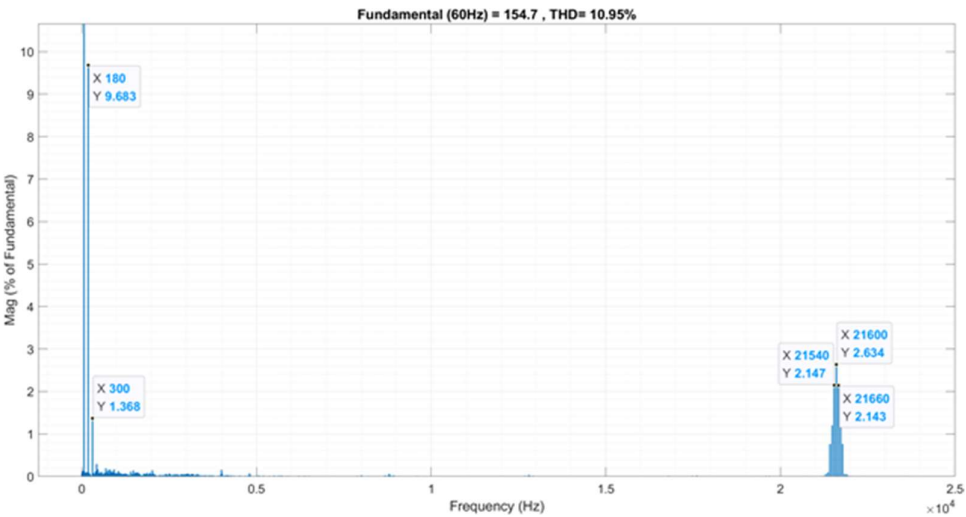
(a)



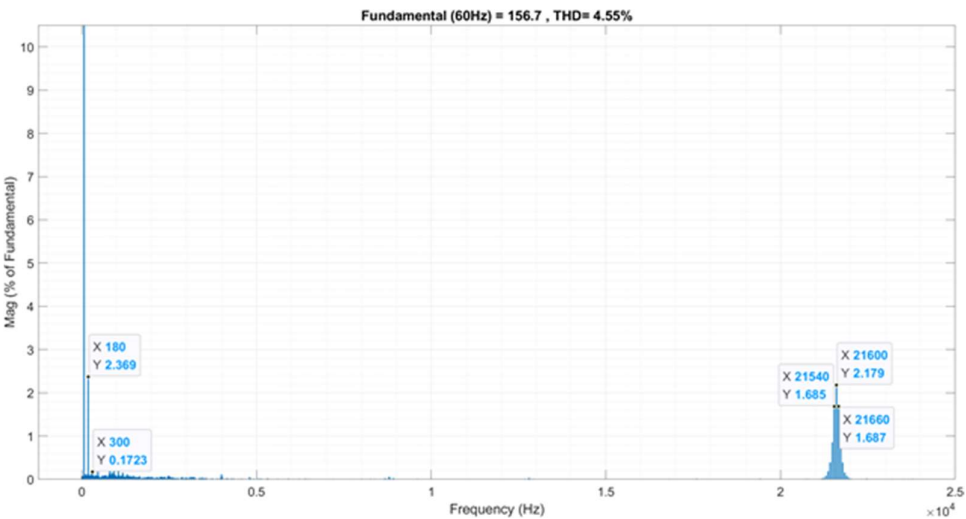
(b)

Figure 16. The hardware results’ of the voltage and current output waveforms using (a) traditional SPWM control; (b) modified SPWM control

In addition, this study also analyzed the THD of the AC voltage output with simulations, where the AC voltage output was the voltage difference between two capacitors and the voltage capacitor changes along with the switching frequency. Therefore, the THD was also affected by the switching frequency. Figure 17 shows the simulation analysis of the THD. In Figure 17(a), (b), the THD of the traditional SPWM control is 10.95% while the THD of the modified SPWM is lower at 4.55%. The reason is related to the aforementioned phenomenon shown in Figure 15, 16.



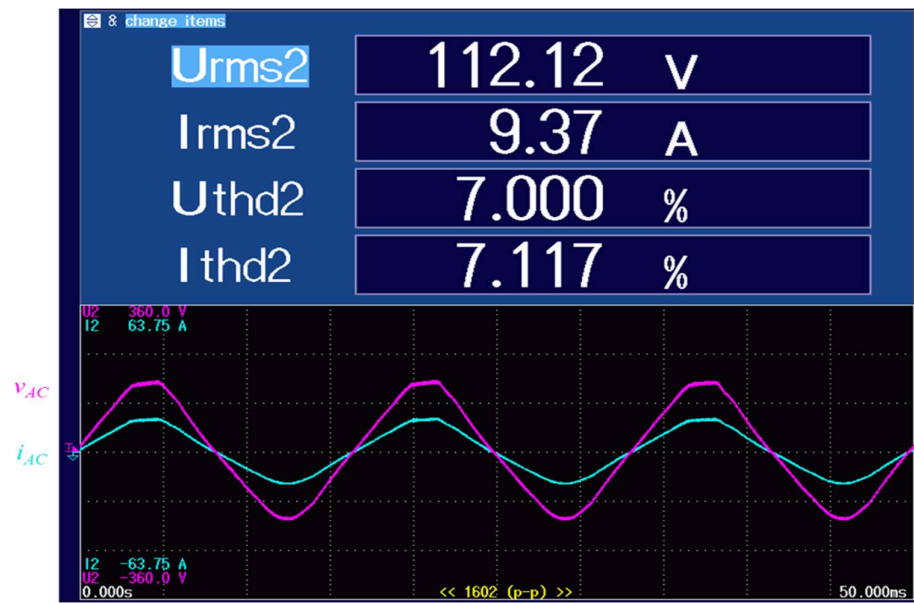
(a)



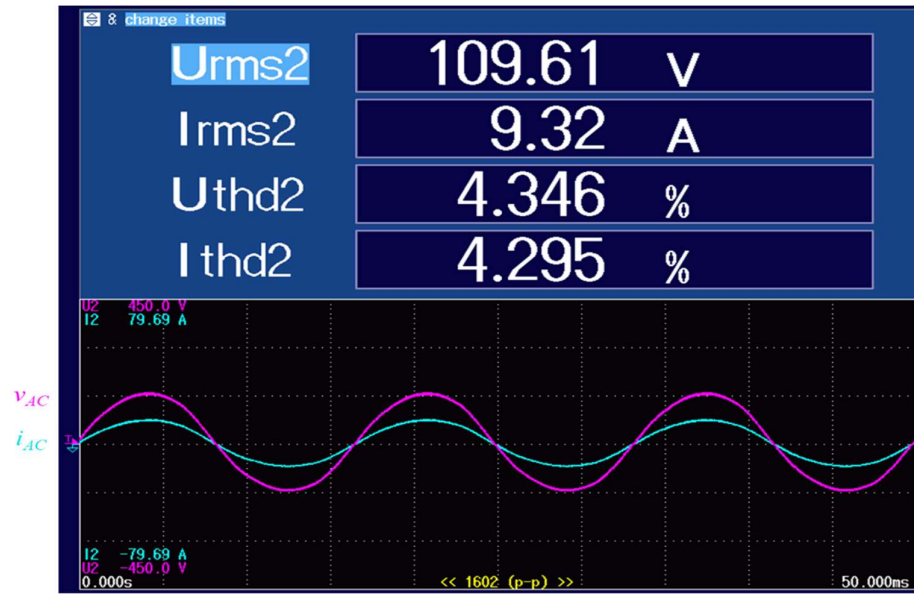
(b)

Figure 17. Simulation’s THD analysis using (a) traditional SPWM control; (b) modified SPWM control

Finally, the actual experiments were implemented by the hardware shown in Figure 12. The THD analysis of the AC output voltage was obtained by the Power Analyzer. The results are shown in Figure 18, where the THD of the traditional SPWM control is 7% while the THD of the modified SPWM is lower at 4.346%. The results are within the standard, which gives 5% limitation in IEEE Std 519-1992 and 8% in IEEE Std 519-2014, respectively[19].



(a)



(b)

Figure 18. Hardware experiment’s THD analysis using (a) traditional SPWM control; (b) modified SPWM control

5. Conclusions

This study replaced the traditional BESS topology with a single-stage topology based on the SSDBI, which reduced component counts and system complexity, and increased the power density. In addition, a modified SPWM control was raised to improve the THD of the proposed inverter. The modified SPWM control decreased the THD from 10.95% to 4.55% in simulations, from 7% to 4.34% in actual measurements instead of other complex control. Through the modified SPWM control, the proposed inverter can operate safely and stably and comply with IEEE Std 519-1992 and IEEE Std 519-2014 standards.

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