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Non-Isolated Ultra-High Step-Up DC-DC Converter Topology Using Coupled-Inductor Based Inverting Buck-Boost and Voltage Multipliers

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Abstract: This paper introduces a non-isolated ultra-high voltage gain topology using the combination of the coupled-inductor-based inverting buck-boost converter (IBB) and voltage multiplier (VM) structure. In the proposed converter, an ultra-high step-up voltage gain can be achieved with a small duty cycle thanks to a coupled inductor and VMs. The voltage stress and the losses of the switches in the proposed converter are even less compared to other conventional topologies. Unlike other coupled-inductor topologies, a large voltage spike caused by the leakage inductance of the coupled inductor is smoothed by the capacitor in the voltage multiplier. In addition, ZVS turn-on for the switches and ZCS turn-off for the diodes can be achieved with the energy stored in the leakage inductance. A 360W (40V/380V) prototype converter is implemented to prove the advantages of the proposed converter, with a maximum efficiency of 98.4%.

Keywords: coupled inductor; inverting buck-boost; non-isolated dc–dc converters; ultra-high step-up; ultrahigh voltage gain; voltage multiplier

1. Introduction

Nowadays, renewable energy sources such as fuel cells (FCs) and photovoltaic (PV) modules have become important energy sources which can replace fossil fuels. However, due to their low output voltage characteristics, normally ranging from 24V to 48V, it is necessary to boost the voltage up to 380V, which is suitable for the DC link of a single-phase or 700V for a three-phase grid-tie inverter [1].

The simplest way to achieve high step-up voltage gain is by using an isolated converter by adjusting the turns ratio of the transformer. However, due to their disadvantages of high losses, large volume, and high cost, since a greater number of turns for the transformer is required, they are not a suitable choice for applications that do not require isolation between input and output [17].

Conventional non-isolated boost converters could be a candidate. However, in order to achieve high step-up voltage gain, they have to work with an extreme duty cycle, which leads to decreased efficiency and increased system cost since high voltage rating components have to be used due to high voltage stress [2].

Recently, many high step-up voltage gain topologies have been introduced [3–38]. They can be divided into two groups: single-inductor based converters [4–14] and coupled-inductor based converters [16–38]. Single-inductor based converters include interleaved boost or buck-boost converters [4–6], switched-inductor and voltage lift techniques [7,8,11,12], voltage multiplier (VM) and their combination topologies [13–15]. These types of converters can achieve higher step-up voltage gain than conventional ones with high efficiency. However, for an ultra-high step-up voltage ratio, more converter stages must be cascaded, resulting in the use of more components, which decreases efficiency and increases volume and cost.

Coupled-inductor based topologies can easily meet the high step-up voltage gain requirement by adjusting the turns ratio of the coupled inductor. However, there are still some issues that need to

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be solved to achieve high efficiency, high power density, and low cost, high turns ratio and leakage inductance of the coupled inductor, switching losses, and voltage stress on components.

The first issue is the high turns ratio of the coupled inductor, which leads to increased inductor volume and winding resistance, thereby reducing the power density and efficiency of the system. Moreover, the leakage inductance causes a very high voltage spike applied to the switches, resulting in high power losses and the need for high voltage rating components, thereby increasing the cost. The leakage inductance problem can be solved by using a passive snubber [16–28,33], or an active snubber [29–32], or passive clamping [36,37] so low voltage rating switches can be used with low internal resistance $R_{ds(on)}$, hence increasing the overall efficiency. However, this requires more components, increases control complexity for the active snubber, and consequently increases the losses, volume, and cost of the converter.

Another issue that mainly affects the efficiency of the converter is switching losses. Even though the voltage spike applied to the switches caused by leakage inductance is eliminated, the efficiency of the converters in [16,18,31] is still low because of hard switching, resulting in high switching losses in the switches. Moreover, these losses are proportional to the increase in switching frequency. So, in order to maintain efficiency, the converter must work at a low switching frequency, which leads to larger required values for the capacitor and inductor, thus decreasing the power density. The topologies introduced in [21,23,24,26,27,29,30,32,33,35,36] can achieve soft switching to improve efficiency. In these converters, the snubbers or clamped circuits not only eliminate the voltage spike applied to semiconductor devices by absorbing the energy of the leakage inductance but also use this energy to provide Zero-Voltage Switching (ZVS) or Zero-Current Switching (ZCS) for the switches and diodes.

The third issue that increases the volume and cost of the converter is the voltage stress on components. Because of the asymmetrical configuration, the voltage stress on components in converters proposed in [16–35,37,38] are not evenly distributed. The components on the output side have higher voltage stress. So, all of them need to have higher voltage ratings, leading to increased volume and cost of the system. For example, the converter in [18] has voltage stress on output capacitor equal to output voltage and voltage stress on output diode is nearly equal to the output voltage. Similarly, the converter in [21] has the voltage stress on output diode nearly equal to output voltage.

In order to overcome all of these issues, the proposed converter has been introduced with the following features:

- Ultra-high step-up voltage gain with a low turns-ratio of the coupled inductor.
- ZVS turn-on for switches and ZCS turn-off for all diodes
- No voltage spike problem caused by leakage inductance without using an extra snubber circuit.
- Low voltage stress on all components due to the symmetrical configuration.
- Flexibly achieving higher step-up voltage gain with low duty cycle by either adjusting the turns ratio of coupled inductor or cascading a greater number of VM stages.

This paper is divided into six sections. The working principle of the proposed converter is presented in Section 2. The design procedure of the proposed converter is presented in Section 3. In Section 4, the experimental results demonstrating the superiority of the proposed converter are discussed. The comparison between the proposed converter and other topologies is shown in Section 5. Finally, the conclusion is in Section 6.

2. Proposed Converter Structure

2.1. Operating Principle

As shown in Figure 1, the proposed topology consists of two voltage multipliers (VM): positive VM (which includes diodes D_1, D_2 and capacitors C_1, C_s) and negative VM (which includes diodes D_3, D_4 and capacitors C_3, C_D) connected to the synchronous Inverting Buck-Boost (IBB) converter.

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Moreover, the main inductor of IBB is replaced by a coupled inductor, and the secondary side of the coupled inductor is placed at the common path between two blocking capacitors C_s and C_D of the positive VM and negative VM, respectively, not only for creating the ZVS turn-on for switches and ZCS turn-off for diodes but also to increase the overall voltage gain of the proposed converter. In the proposed topology, the leakage inductance referred to the secondary side is used for the ZVS condition, and its energy is absorbed by blocking capacitors C_s and C_D. Hence, no snubber is needed in the proposed topology. Furthermore, symmetrical configuration ensures that the voltage stress and current stress are evenly shared among all output components. Consequently, low-cost and small-volume components with low voltage ratings can be used.

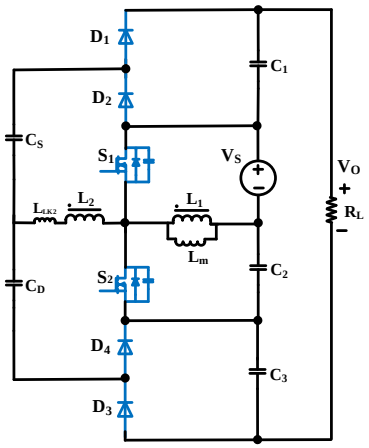

Figure 1. The Proposed Converter.

In this section, the working principle of the proposed converter is described in Continuous Conduction Mode (CCM). From the key waveform shown in Figure 2, one switching cycle is divided into six modes based on the working status of the main switches. The equivalent circuit for each mode is shown in Figure 3. In the proposed two-stage converter, the main switches and the synchronous rectifier switches are synchronized in operation. To describe the operating principle of the proposed converter, the following assumptions are made:

- The circuit is operating in steady state mode, and the magnetizing inductor current is continuous.
- All the components are ideal, and the parasitic components are neglected.
- All the capacitors are large enough to maintain their voltages constant during a switch-off period.
- All the output capacitors have the same value ($C_1 = C_2 = C_3$), and all the blocking capacitors have the same value ($C_S = C_D$).
- The switching period is T_s; the switch S_1 is closed for time DT_S and open for time (1-D) T_s and vice versa.
- The turns ratio of the coupled inductor and the relationship between the voltage of each winding are defined in (1)

$$N = \frac{N_2}{N_1} \quad , \qquad V_{L_2} = \frac{N_2}{N_1} V_{L_1} \tag{1}$$

where: N is turns-ratio, N_1 and N_2 are the number turns of primary and secondary winding, respectively. V_{L_1} and V_{L_2} are voltage of the primary and secondary winding of the coupled inductor.

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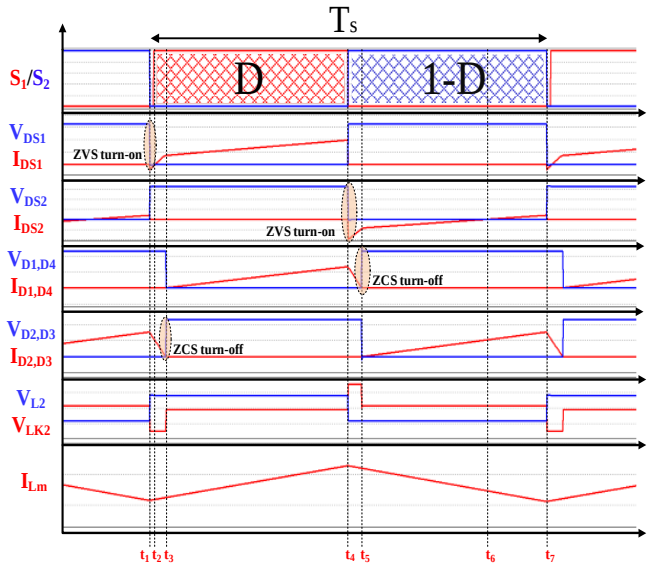

Figure 2. Key waveforms of the proposed converter under CCM.

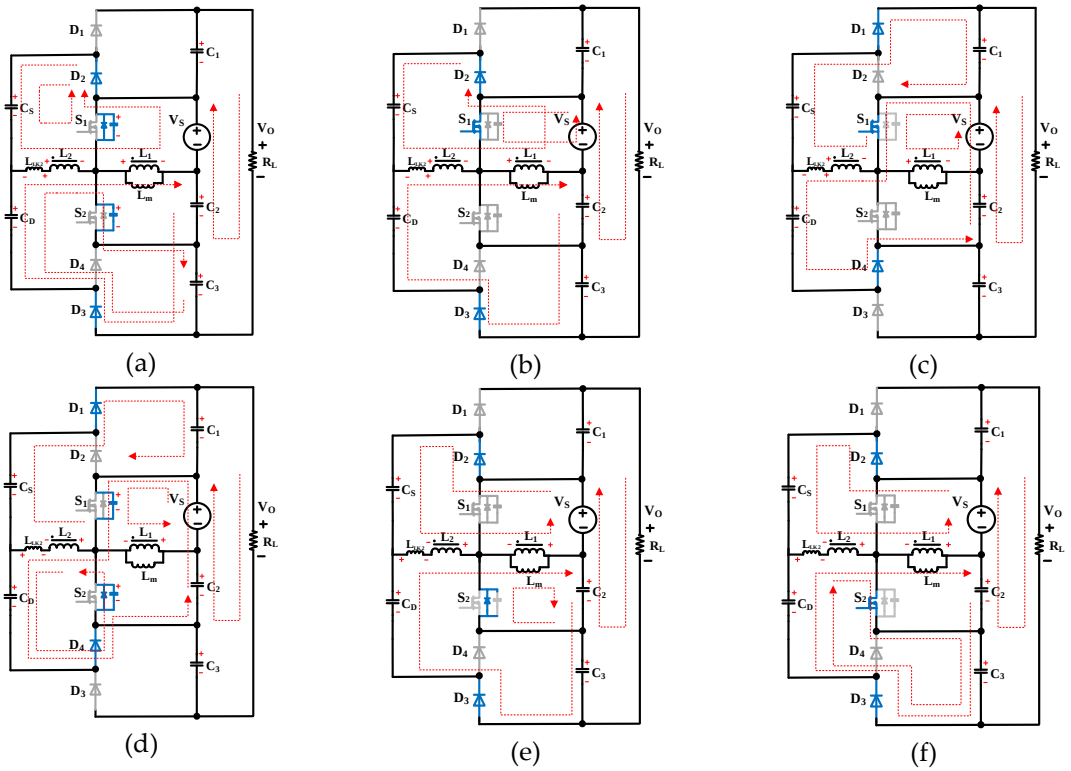

Figure 3. Equivalent circuit of each mode of operation in the proposed converter under CCM: (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e)Mode 5, (f) Mode 6.

Mode 1 (t_1-t_2)

Before t_1, S_1 is off, D_1 and D_4 are reverse biased and S_2, D_2 and D_3 were conducting. At $t = t_1$, S_2 turns off, the parasitic capacitor C_{oss1} of S_1 is discharged. The coupled inductor starts to charge. Due to the charging of the parasitic capacitor C_{oss2} of S_2 and the discharging of leakage inductor L_{LK2}, the voltage across S_2 is raised up and the body diode of S_1 is forward biased to create the ZVS turn-on for S_1.

Mode 2 (t_2-t_3)

At $t = t_2$, S_2 is off, the parasitic capacitor of S_2 is fully charged and that of S_1 is fully discharged. S_1 turns on with ZVS condition as created from Mode 1. Since the S_1 is fully on, its body

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diode is reverse biased, hence the current will flow through S_1 instead of its body diode. At the end of this mode, the L_{LK2} is fully discharged, the current through the diodes D_2 and D_3 decrease to zero and ZCS turn-off for these diodes is achieved.

Mode 3 (t_3-t_4)

At $t = t_3$, S_1 is on, and S_2 is off, and the coupled inductor is being charged. Due to the secondary winding voltage of the coupled inductor, D_1 and D_4 are forward biased, D_2 and D_3 are reverse biased, causing capacitors C_D and C_1 are discharged, C_s is charged. During this mode, the leakage inductor L_{LK2} stores the energy.

By using Kirchhoff's Voltage Law (KVL), the equation expression in this mode can be expressed as follows.

$$V_{L_1} = V_S, V_{L_2} = NV_{L_1} = NV_S \tag{2a}$$

$$V_{C_S} + V_{L_2} = V_{C_1} + V_{L_{LK2}} \tag{2b}$$

$$V_{L_1} + V_{L_2} + V_{C_2} = V_{C_D} + V_{L_{LK2}} \tag{2c}$$

$$V_O = V_{C_1} + V_{C_2} + V_{C_3} + V_S \tag{2d}$$

By using Kirchhoff's Current Law (KCL), the current I_{LLK2} of leakage inductor L_{LK2} can be calculated as in (3).

$$I_{L_{LK2}} = \frac{C_1 \Delta V_{C1}}{(t_4 - t_3)} + \frac{V_{L_1}(t_4 - t_3)}{NL_1} + \frac{C_2 \Delta V_{C2}}{(t_4 - t_3)} \tag{3}$$

Since the output current ripple is very small and can be neglected, the voltage of capacitor C_3 can be considered constant. Then the total ripple of the output voltage is only contributed by the voltage ripple of capacitors C_1 and C_2. Moreover, from the earlier assumption, capacitors C_1, C_2, and C_3 have the same value. Then the leakage inductor current can be rewritten as follows.

$$I_{L_{LK2}(t_4 - t_3)} = \frac{2C_1 \Delta V_O}{(t_4 - t_3)} + \frac{V_{L_1}(t_4 - t_3)}{NL_1} \tag{4}$$

And the voltage of the leakage inductor in this mode can be calculated as follows.

$$V_{L_{LK2}(t_4 - t_3)} = \frac{L_{LK2} di_{L_{LK2}}}{dt} = \frac{L_{LK2}\left(2C_O \Delta V_O NL_1 + V_{L_1}(t_3 - t_2)^2\right)}{(t_3 - t_2)^2 NL_1} \tag{5}$$

Mode 4 (t_4-t_5)

At $t = t_4$, S_1 turns off, S_2 turns on. The diodes D_2 and D_3 are reverse biased, D_1 and D_4 are forward biased. The body diode of S_2 is forward biased and conducted, the parasitic capacitor C_{oss2} of S_2 is discharged and the parasitic capacitor C_{oss1} of S_1 is charged. The coupled inductor and leakage inductor L_{LK2} start to discharge. Due to the discharging of leakage inductor L_{LK2}, the currents through diodes D_1 and D_4 are decreased and create ZCS turn off for these diodes. At the end of this mode, the leakage inductor L_{LK2} is fully discharged.

Mode 5 (t_5-t_6)

In this mode, the energy stored in the core of coupled inductor is discharged to the output capacitor C_2, and the blocking capacitor C_D of negative VM is discharged to the output capacitor C_3. The secondary side leakage inductor L_{LK2} is charged after being fully discharged in Mode 3. The blocking capacitor C_s of positive VM is charged for the next discharging cycle. The voltage applied to capacitor C_s is not only the input voltage but also the voltage of primary and secondary winding of coupled inductor minus the voltage drop on leakage inductor L_{LK2} while it is charging. Similarly, the voltage applied to the output capacitor C_3 is not only the voltage of blocking capacitor C_D but also the voltage of secondary winding of coupled inductor resulting in the increasing of the overall voltage gain of proposed converter without increasing the voltage stress on components.

By using KVL, the equations of this mode can be expressed as in (6).

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$$V_L = V_{C_2}, V_{L_2} = NV_{L_1} = NV_{C_2} \tag{6a}$$

$$V_{L_1} + V_{L_2} + V_S = V_{C_S} + V_{L_{LK2}} \tag{6b}$$

$$V_{C_D} + V_{L_2} = V_{C_3} + V_{L_{LK2}} \tag{6c}$$

$$V_O = V_{C_1} + V_{C_2} + V_{C_3} + V_S \tag{6d}$$

Mode 6 (t_6-t_7).

At $t = t_6$, the voltage of the capacitor C_2 is raised up higher to the primary winding voltage of the coupled inductor, the body diode of S_2 reverse biased. Hence the current flows through S_2 instead of its body diode. At the end of this mode $t = t_7$, one switching period is done, everything is ready for the next cycle.

The leakage inductor L_{LK2} is charged in whole time of Mode 5 and Mode 6. Similar in Mode 3, the current I_{LLK2} flow through the leakage inductor L_{LK2} can be calculated as in (7) by using KCL.

$$I_{L_{LK2\_(t_7-t_5)}} = \frac{2C_1\Delta V_o}{(t_7 - t_5)} + \frac{V_{L_1}(t_7 - t_5)}{NL_1} \tag{7}$$

Hence, the voltage of the leakage inductor L_{LK2} in this mode can be calculated as follows.

$$V_{L_{LK2}(t_7-t_5)} = \frac{L_{LK2}di_{L_{LK2}}}{dt} = \frac{L_{LK2}\left(2C_O\Delta V_O NL_1 + V_{L_1}(t_7-t_5)^2\right)}{(t_7-t_5)^2 NL_1} \tag{8}$$

2.2. Steady State Analysis of the Proposed Converter

2.2.1. Voltage Gain and Voltage Stress on Components

Since Mode 1, Mode 2 and Mode 4 occur in a very short period of time, we can neglect these three modes in steady-state analysis. Hence, the period $(t_2 - t_4)$ will be DT_S and period $(t_7 - t_5)$ will be $(1 - D)T_S$. Applying the voltage-second balance, the following equations can be obtained as in (9),

$$\bar{V}_{L_1} = DV_S - (1 - D)V_{C_2} = 0 \tag{9a}$$

$$\bar{V}_{L_1} = DV_S - (1 - D)\left(V_{C_S} + V_{L_{LK2}(t_7-t_5)} - NV_{C_2} - V_S\right) = 0 \tag{9b}$$

$$\bar{V}_{L_1} = D(V_{C_D} + V_{L_{LK2}(t_4-t_3)} - NV_S - V_{C_2}) - (1 - D)V_{C_2} = 0 \tag{9c}$$

$$V_O = V_{C_1} + V_{C_2} + V_{C_3} + V_S \tag{9d}$$

Hence, the voltage of capacitors can be calculated by using (10).

$$V_{C_2} = \frac{DV_S}{1 - D} \tag{10a}$$

$$V_{C_D} = \left(N + \frac{1}{1 - D}\right)V_S - \frac{L_{LK2}\left(2C_1\Delta V_o NL_1 + V_{L_1}(DT_s)^2\right)}{NL_1(DT_s)^2} \tag{10b}$$

$$V_{C_S} = \left(\frac{1 + ND}{1 - D}\right)V_S - \frac{L_{LK2}\left(2C_1\Delta V_o NL_1 + V_{L_1}((1 - D)T_s)^2\right)}{NL_1((1 - D)T_s)^2} \tag{10c}$$

$$V_{C_1} = V_{C_3} = \left(\frac{1 + N}{1 - D}\right)V_S - \frac{L_{LK2}\left(2C_1\Delta V_o NL_1 + V_{L_1}((1 - D)T_s)^2\right)}{NL_1((1 - D)T_s)^2} - \frac{L_{LK2}\left(2C_1\Delta V_o NL_1 + V_{L_1}(DT_s)^2\right)}{NL_1(DT_s)^2} \tag{10d}$$

And the output voltage equation can be derived as in (11).

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$$V_o = \left(\frac{3+2N}{1-D}\right)V_S - \frac{2L_{LK2}\left(2C_1\Delta V_o NL_1 + V_{L_1}((1-D)T_s)^2\right)}{NL_1((1-D)T_s)^2} - \frac{2L_{LK2}\left(2C_1\Delta V_o NL_1 + V_{L_1}(DT_s)^2\right)}{NL_1(DT_s)^2} \quad (11)$$

The voltage stress on semiconductors can be calculated as follows.

$$V_{S_1} = V_{S_2} = \frac{V_S}{1-D} \quad (12a)$$

$$V_{D_1} = V_{D_2} = V_{D_3} = V_{D_4} = V_{C_1} = V_{C_3} \quad (12b)$$

From (11) it is noted that the voltage gain is not only contributed by the VM stages but also by the turns-ratio of the coupled inductor. This means that we can flexibly achieve the ultra-high voltage gain by either cascading more VM stages, increasing the turn-ratio of the coupled inductor or both. Moreover, Equation (12) shows that the voltage stress is shared evenly among the components. Hence the output components will work with low voltage stress. This is an advantage of using the symmetrical configuration mentioned before.

2.2.2. ZVS condition

In Mode 1, to achieve ZVS turn-on for S_1, the voltage of leakage inductor L_{LK2}, while it is discharging, must be larger than the sum of the voltage of blocking capacitor C_s and secondary winding voltage as shown in (13)

$$V_{L_{LK2}} - V_{C_S} - V_{L_2} \geq 0 \quad (13a)$$

$$V_{L_2} = NV_{L_1} = NV_S \quad (13b)$$

The voltage of the leakage inductor can be found from the change of the current through it. As mentioned in Mode 1, the leakage inductor is fully discharged at the end of this mode. So, the change of the current in Mode 1 can be calculated as in (14).

$$\Delta I_{LK2} = I_{LK2(t_1)} - 0 \quad (14)$$

The leakage inductance current at $t = t_1$ actually is the leakage inductance current at $t = t_7$ of the previous switching period and can be derived as in (15).

$$I_{LK2\_(t_1)} = I_{LK2\_(t_7-t_5)} \quad (15)$$

Then the ZVS condition equation can be expressed as in (16).

$$\frac{L_{LK2}\Delta I_{L_{LK2\_(t_7-t_5)}}}{T_r} \geq V_{C_S} + NV_S \quad (16)$$

From (8) and (13), the value of secondary side leakage inductor can be calculated as follows.

$$L_{LK2} \geq \frac{(V_{C_S} + NV_S)T_r}{\Delta I_{L_{LK2\_(t_7-t_5)}}} = \frac{(t_7-t_5)NL_1(V_{C_S} + NV_S)T_r}{2C_1\Delta V_o NL_1 + V_{L_1}(t_7-t_5)^2} \quad (17)$$

As mentioned at the beginning of part B, the period $(t_7 - t_5)$ is denoted by $(1-D)T_S$, then (17) becomes (18).

$$L_{LK2} \geq \frac{(1-D)T_s NL_1(V_{C_S} + NV_S)T_r}{2C_1\Delta V_o NL_1 + V_{L_1}((1-D)T_s)^2} \quad (18)$$

where: T_r is the discharging time of secondary side leakage inductor.

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3. Design of the Proposed Converter

3.1. Design of the Output Capacitors

The output capacitors can be calculated from the maximum allowable output ripple voltage ΔV_O as in (19).

$$C_{Oeq} \geq \frac{I_O D}{f_S \times \Delta V_O} \tag{19}$$

where: f_S is switching frequency, I_o is the output current, and C_{Oeq} is the equivalent output capacitor, that can be calculated as in (20).

$$C_{Oeq} = \frac{C_1 C_2 C_3}{C_1 C_2 + C_2 C_3 + C_3 C_1} \tag{20}$$

To keep the symmetrical configuration, all the output capacitors must have the same value and can be calculated as in (21).

$$C_1 = C_2 = C_3 = 3C_{Oeq} \geq \frac{3I_O D}{f_{SW} \times \Delta V_O} \tag{21}$$

The leakage inductors L_{LK2}, duty cycle D, and the dead time T_d.

Firstly, the minimum duty cycle D_{min} can be calculated from the required voltage gain in the case when the leakage inductor L_{LK2} equals to zero.

$$D_{min} = 1 - (3 + 2N)\frac{V_S}{V_O} \tag{22}$$

The voltage of blocking capacitor C_s in the case of minimum duty cycle D_{min} can be calculated as follows.

$$V_{C_S\_D_{min}} = \left(\frac{1 + ND_{min}}{1 - D_{min}}\right) V_s \tag{23}$$

By using (18) and (23), the minimum required value of leakage inductor L_{LK2} can be calculated with an assumption that the discharging time T_r is equal to the deadtime T_d of switches.

After choosing the value for leakage inductor L_{LK2}, the right value for duty cycle can be found from the output voltage equation shown in (11).

It should be noted that, if the value of the leakage inductor is too large, the voltage gain will be reduced much. Moreover, the S_1 has to be turned on before the leakage inductor L_{LK2} gets fully discharged, then the dead time T_d of switches must be smaller than the discharging time T_r of the leakage inductor L_{LK2} to maintain ZVS condition.

In mode 1, since the body diode of S_1 and D_2 are forward biased, the leakage inductor L_{LK2} will resonate with capacitor C_s. To maintain ZVS condition, the resonant frequency must be much smaller than switching frequency. Moreover, as an assumption before, the capacitors C_s and C_D have the same value to keep the symmetrical configuration, those values can be calculated by using (24).

$$C_S = C_D >> \frac{1}{(2\pi f_S)^2 L_{LK2}} \tag{24}$$

3.2. Design of the Main Inductor

The magnetizing inductance of coupled inductors is designed to operate the proposed converter in CCM mode. Then its value can be calculated as in (25).

$$L_m \geq \frac{V_S D}{\Delta I_{L_m} f_{SW}} \tag{25}$$

where: ΔI_{L_m} is the current ripple of the magnetizing inductor L_m.

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Then, the primary winding inductance L_1 and secondary inductance L_2 can be expressed by using (26).

$$L_1 = L_m + L_{LK1} \tag{26a}$$

$$L_2 = N^2 L_1 \tag{26b}$$

4. Experiment Results

In order to verify the validity of the proposed converter, a 380V, 360W prototype converter is built for a photovoltaic module (Hyundai RI Series 360W, 72 Cell Solar Module). The specifications of the proposed converter are shown on Table 1, and the information about the switches and passive components are shown in Table 2.

In the experiments, the gate signals (V_{GS1}, V_{GS2}) are generated by a DSP TMS320F28335. The prototype converter is shown in Figure 4. All the through-hole components are placed on the top side, the gate drivers are placed on the bottom side. All the capacitors are film capacitors.

The duty cycle of the main MOSFET (S_1) is 0.52 to boost the input voltage 40V to the output voltage of 380V. The deadtime between the two switches is 100ns.

Table 1. Specifications of the Proposed Converter.

Parameter	Designator	Value
Input Voltage	V_S	40 V
Output voltage	V_O	380 V
Maximum Output voltage ripple	ΔV_O	0.8%
Power	P_O	360 W
Switching frequency	f_{SW}	100 KHz

Table 2. Specifications of Components used in the Proposed Converter.

Component	Part #	Specification
MOSFETs	IPP039N10N5	200 V/80 A
Diodes (D_1-D_4)	DSSK10-18A	180 V/10A
Capacitors C_2	106MMR250K	10uF/ 250 V
Turns-ratio of the coupled inductor		17:18
Leakage inductance (L_{LK2})		4.5uH
Primary winding inductance L_1		103uH
Secondary winding inductance L_2		115uH

The experimental results in full load condition are shown in Figure 5. In Figure 5(a), it is clear to see that S_1 is turned on with ZVS condition. The waveform in Figure 5(b) shows the body diode of S_2 is forward biased at the first part of on-time of S_2 (as in Mode 4 of working principal part) and it is reverse biased then the current is changed the direction at the last part of on-time of S_2 (as in Mode 5 of working principal part). Figure 5(c) and (d) show the voltage and current waveforms of the diodes. It is obvious that all the diodes are turned off with ZCS. Figure 6 shows the voltage and current waveforms of switches and diodes in light load (20%) condition. The switch S_1 still achieves ZVS turn-on, and the diodes still achieve ZCS turn-off as in full load condition. It is strong evidence to show the proposed converter can achieve ZVS turn on for switches and ZCS turn-off for diodes in the whole range of load. It should be noted that the oscillation of current when switches are off is

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observed because of a small snubber capacitor used to eliminate the hot-loop issue in half-bridge configuration.

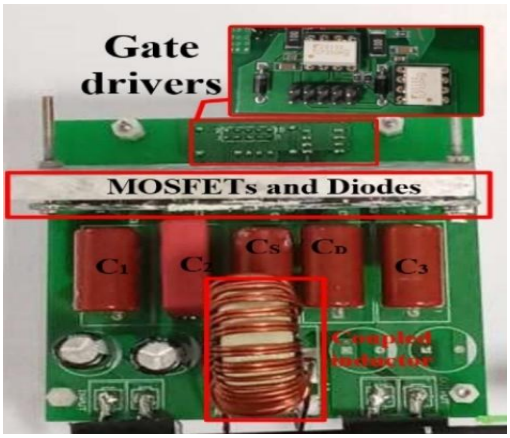

Figure 4. Prototype of the proposed converter.

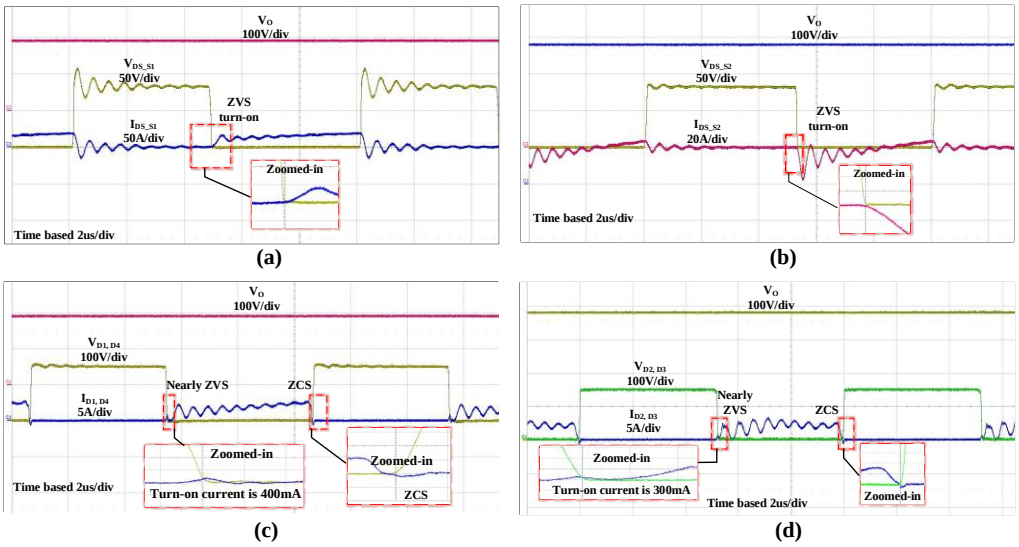

Figure 5. Experimental waveforms of the prototype converter with 100% load: (a) MOSFET S_1, (b) MOSFET S_2, (c) Diodes D_1 and D_4, (d) Diode D_2 and D_3.

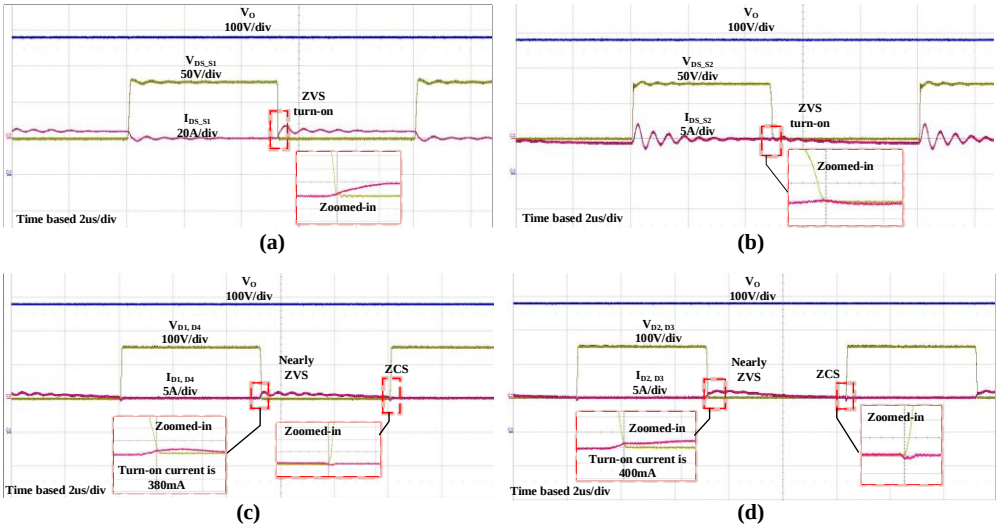

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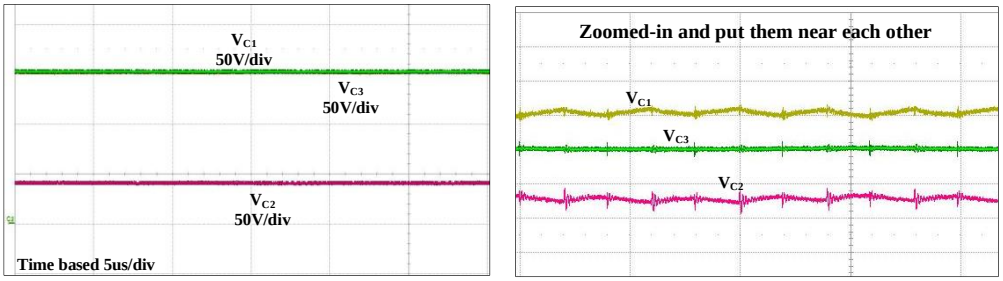
Figure 6. Experimental waveforms of the proposed converter under light load conditions (20% load): (a) MOSFET S_1, (b) MOSFET S_2, (c) Diodes D_1 and D_4, (d) Diode D_2 and D_3.

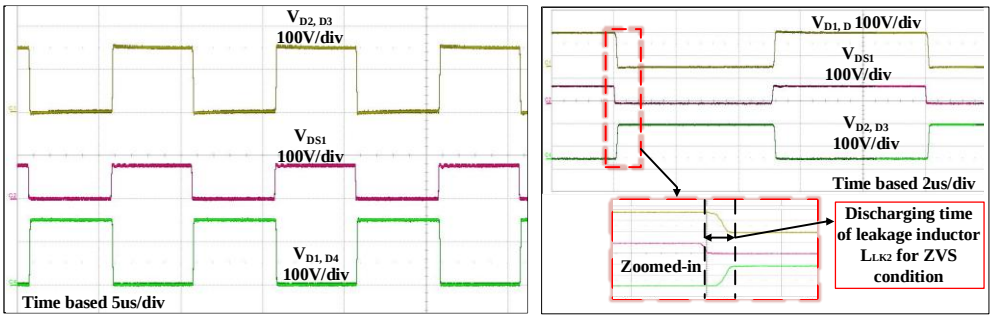
Figure 7 shows the waveforms of output capacitors. Due to the symmetrical configuration, the voltage of output capacitors C_1 and C_3 of two voltage multiplier stages are the same. And the voltage of the IBB output capacitor C_2 is lower as compared to those of voltage multipliers as a result of the small duty cycle. Moreover, from Figure 7(b), it shows that the capacitors C_1 and C_2 are interleaved with each other, then their voltage ripples will be canceled out each other and then contribute to the low voltage ripple for output voltage. Hence the smaller value output capacitor can be used to achieve the required output voltage ripple.



(a) (b)

Figure 7. (a) Experimental voltage waveforms of output capacitors, (b) Zoomed in waveforms of output capacitors voltage.

Figure 8(a) shows the voltage waveforms of the diodes and MOSFET S_1. These waveforms are exactly matched with the simulation. In Figure 8(b) zoomed in voltage waveforms of diodes and MOSFET S_1, it is observed that the MOSFET S_1 is turned on before the diodes D_1 and D_4 turn on, and D_2 and D_3 turn off, at the period of 160ns, which is 60ns longer than the dead time of switches. This is the required time to achieve ZVS turn-on for S_1 and ZCS turn-off for diodes as explained before in Part II.



(a) (b)

Figure 8. (a) Experimental voltage waveforms of diodes and MOSFET S_1, (b) zoomed-in voltage waveforms of diodes and MOSFET S_1.

Figure 9 shows the waveforms of coupled inductors at full load. It can be noted that the leakage inductor L_{LK2} is discharging causing high voltage spikes in secondary winding of the coupled inductor in a small period of time before the voltage of the coupled inductor changes its polarity. It is another requirement for ZVS turn-on for S_1 and ZCS turn-off for the diodes.

A Power analyzer (Xitron 2802) is used for measuring the converter efficiency. Figure 10 shows the measured efficiency plot of the proposed converter when V_S = 40 V, V_O = 380V and f_{sw}=100 kHz.

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As shown in Figure 10, efficiency achieves 97% at light load (20% load) and 96% at heavy load (100% load). The maximum efficiency of 98.4% is obtained at 150W.

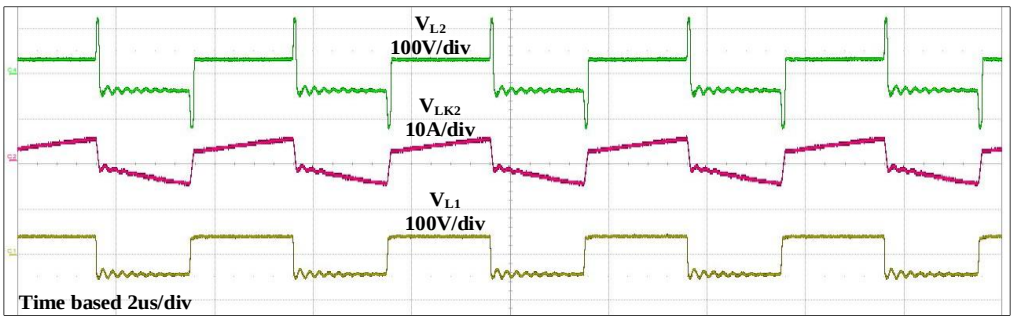

Figure 9. Measured waveforms of the coupled inductor voltage and current.

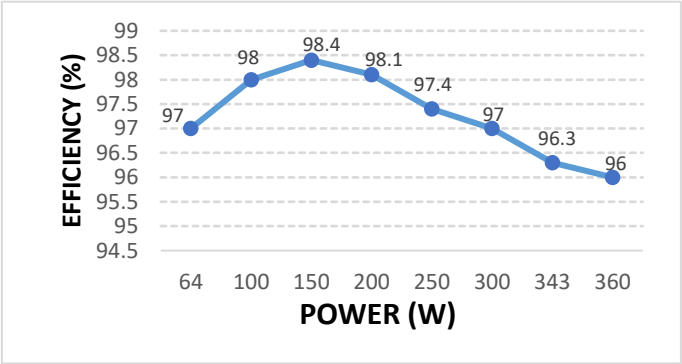

Figure 10. Measured efficiency curve of proposed converter.

5. Comparison Study

The comparison between the proposed converter and other converters is shown in Table 3. From Table 3, it is clear that the proposed converter has the highest efficiency with a low voltage stress on components and a low number of components. The voltage gain comparison is shown in Figure 11 for the turns-ratio of 1.05. The converters in [16,21,31,34,36–38] have higher voltage gain than the proposed topology. However, the voltage stress on output diodes and capacitors is much higher, and the efficiency is much lower than that of the proposed converter. Therefore, it can be concluded that the proposed converter has superior advantages compared to other new topologies. Moreover, the converters in [21,31,34] have a small range of duty cycle, from 0.1 to 0.5. Thus, with applications requiring several hundred watts and very high step-up voltage conversion, the current stress on components will increase significantly, leading to a reduction in the efficiency of the converter. From Figure 12, the comparison of the graphs of stress on diodes with different converters is shown with the proposed converter.

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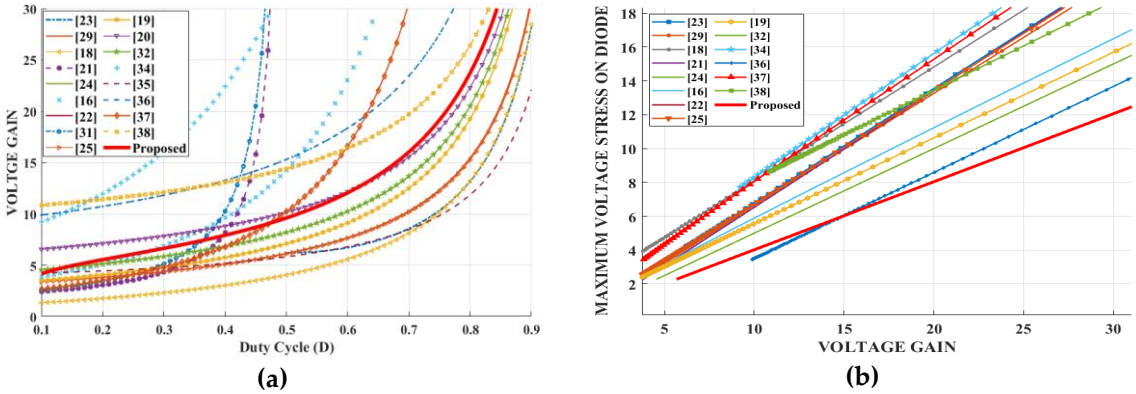

(a) (b)

Figure 11. (a) Voltage gain graph (b) Maximum voltage stress on diodes graph.

Table 3. Comparison of proposed converter with other existing topologies.

Topology	Voltage gain $M = \frac{V_o}{V_{in}}$	Voltage stress on switches (Vs/Vin)	Maximum voltage stress on diodes (VDmax/Vin)	Maximum voltage stress on output capacitors (VCo/Vin)	S/D/CI/I/C/T	Efficiency
[23]	$\frac{(2N+1)(1-2D+2D^2)}{D(1-D)}$	$\frac{(1-2D+2D^2)}{D(1-D)}$	$\frac{2N(1-2D+2D^2)}{D(1-D)}$	NI	2/3/2/0/5/12	96.5%
[29]	$\frac{D(N-1)+N+2}{(1-D)}$	$\frac{1}{1-D}$	$\frac{N+1}{1-D}$	$\frac{2}{1-D}$	2/3/1/1/5/12	96.8%
[18]	$\frac{1+(N+1)D}{(1-D)}$	$\frac{1}{1-D}$	$\frac{N+1}{1-D}$	$\frac{1+(N+1)D}{(1-D)}$	1/2/1/1/3/8	94.1%
[21]	$\frac{1+N(1-D)}{1-2D}$	$\frac{1}{1-2D}$	$\frac{N}{1-2D}$	$\frac{N(1-D)}{1-2D}$	2/2/1/1/4/10	95.6%
[24]	$\frac{2+2N}{1-D}$	$\frac{1}{1-D}$	$\frac{1+N}{1-D}$	NI	2/6/2/0/6/16	96.7%
[16] (Figure 4a)	$\frac{2+N+DN}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	$\frac{N+1}{(1-D)^2}$	$\frac{N+1}{(1-D)^2}$	1/6/1/1/5/14	94.4%
[22]	$\frac{2+2N}{1-D}$	$\frac{1}{1-D}$	$\frac{1+N}{1-D}$	$\frac{1+2N-ND}{1-D}$	1/4/1/0/4/10	97.1%
[31] (Figure 6b)	$\frac{N+1}{1-2D}$	$\frac{1}{1-2D}$	NI	$\frac{N}{1-2D}$	1/4/1/1/5/12	95%
[25] (Figure 4)	$\frac{N+2}{1-D}$	$\frac{1}{1-D}$	$\frac{N+1}{1-D}$	$\frac{N+2}{1-D}$	1/3/1/0/3/8	96.4%
[19]	$\frac{N+2+D}{1-D}$	$\frac{1}{1-D}$	$\frac{N+1}{1-D}$	$\frac{N+2+D}{1-D}$	1/4/1/1/5/12	96.2%
[20]	$\frac{4+N(2-D)-D}{1-D}$	$\frac{1}{1-D}$	$\frac{N(2-D)-D}{1-D}$	$\frac{4+N(2-D)-D}{1-D}$	1/8/1/0/8/18	97.6%
[32]	$\frac{2(1+N)}{1-D}$	$\frac{1}{1-D}$	$\frac{(1+N)}{1-D}$	$\frac{(1+N)}{1-D}$	2/4/1/0/5/12	96.3%
[34]	$\frac{(N^2+(1+N)(3+D)}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	$\frac{(2+N)}{(1-D)^2}$	NI	2/5/2/5/14	95.2%
[35]	$\frac{2+2N+ND(1-D)}{(1-D^2)}$	$\frac{1}{(1-D)^2}$	$\frac{N(2-D)}{(1-D)}$	$\frac{(1+2N-ND)}{2+2N+ND(1-D)}$	2/5/1/1/5/14	94.2%
[36]	$\frac{5-2ND+4N-D}{(1-D)}$	$\frac{1}{(1-D)}$	$\frac{K(N+1)}{1-D}$	NI	2/8/2/0/8/20	94.6%
[37]	$\frac{1+N+D}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	$\frac{1+N}{(1-D)^2}$	$\frac{1+N}{1+N+D}$	2/4/2/0/4/12	94.4%
[38]	$\frac{((8N+2)+2D(1-4N))}{(1-D)}$	$\frac{1}{(1-D)}$	$\frac{2N(4-3D)}{(1-D)}$	NI	2/5/3/0/5/15	95.96%
Proposed converter	(11)	$\frac{1}{1-D}$	(10d)	(10d)	2/4/2/0/5/13	98.4%

With S/D/CI/I/C/T: Switch/Diode/Coupled Inductor/Single Inductor/Capacitor/Total, N: turns ratio of coupled inductor, NI: No Information.

6. Conclusions

In this paper an ultra-high step-up converter using coupled inductor with low voltage stress on components and high efficiency while achieving a high step-up voltage gain characteristic is proposed. The proposed topology is advantageous in terms of the following features:

- No spike voltage applied to semiconductor devices and hence no need for extra snubber.

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- Very high efficiency with ZVS turn-on for MOSFET and ZVZCS for diodes.
- Reduced voltage stress on the components due to the symmetric configuration.
- Easy to get higher voltage gain by either choosing turns ratio of coupled inductor, duty cycle or cascading more VM stages.

The proposed converter can be a very good choice for ultra-high voltage step-up applications such as the distributed power generation systems with renewable energy sources, which requires a high voltage gain without using a transformer.

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