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Article

Stability, Mounting, and Measurement Considerations for a 20W and 25% Power Added Efficiency 2-10 GHz High-Power Amplifier for Multifunction RF Systems Manufactured in Leonardo's GaN pHEMT 0.25 μm Technology

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Abstract: A high-performance broadband High Power Amplifier (HPA) has been developed employing 250 nm gate length Gallium Nitride (GaN) technology from the **LEONARDO** foundry GN25. This HPA employs the a corporate configuration for FET transistors, optimizing its performance. This article provides an in-depth study and analysis of the critical design parameters of such HPAs in Monolithic Microwave Integrated Circuit (MMIC) technology. The designed MMIC chip measures $7.5 \times 7 \text{ mm}^2$ and includes three stages, each carefully optimized to maximize efficiency and performance. Both the design and the measurement results of amplifier are presented. The most remarkable feature of this chip is an operational bandwidth exceeding two octaves, covering a wide RF frequency range from 2 to 10 GHz (2.23:1 ratio). Additionally, the amplifier achieves an output power higher than 43 dBm, along with a power-added efficiency (PAE) surpassing 20% in the mentioned frequency range (2-10 GHz). This HPA is suitable to be integrated into future Transmit and Receive Modules (TRMs) for Active Electronically Scanned Array (AESA) systems. These systems include multiple capabilities in a single device, such as Radar, Electronic Warfare (EW), and Communications (COMMs) functions, demonstrating the versatility and high efficiency of this design in advanced multifunctional applications.

Keywords: MMIC; broadband amplifier; GaN; PAE; HPA; stability analysis

1. Introduction

Nowadays, equipment designed for military applications, such as communications or electronic warfare (EW), is experiencing a significant increase in relevance, largely due to the various conflicts that have arisen on the global stage [1,2]. Multifunctional RF systems (MFRF) that integrate multiple RF functions such as radar, electronic warfare (EW) or communications (COMMs) in a single system are of particular interest today [3–6]. To achieve this capability, active electronically scanned array (AESA) systems are an essential technology. In this regard, the CROWN Project represents an initial stage in the development of a fully European AESA with combined radar, COMMs, and EW functions. The main objective of the CROWN Project is to demonstrate the integrated and coordinated operation of the different functions (Radar, EW, COMMs) in a digital RF AESA system [7–9]. The project is being carried out by the main representatives of the European defense industry. In total, 11 entities from 7 European countries.

AESA systems are based on an array of antennas with a transmission (Tx) and reception (Rx) module connected to each of the radiating elements. These Tx/Rx modules consist on a high-power amplifier (HPA) in Tx mode and a low-noise amplifier (LNA) in Rx mode. To switch between Tx and Rx

modes single-pole double-throw (SPDT) switches are included to provide this capability. Additionally, beamforming elements are placed in each channel, such as a phase shifter or a real-time delay circuit (TTD), to generate the required phase shift enabling electronic scanning capabilities. The HPA, LNA, and beamforming elements are typically packaged in monolithic microwave integrated circuit (MMIC) modules that are placed into the array structure to be as close as possible to the radiating elements, minimizing system losses.

In the space and military electronics industry, the use of Gallium Arsenide (GaAs) technology for implementing various subsystems has become well-established, largely due to the following characteristics: low noise level, high operating frequency, moderate power level, and excellent immunity to radiation interference [10–14]. However, in the defense and satellite domains, even more demanding requirements needed, requiring receivers with superior robustness and the ability to handle even higher power levels [15–18]. The robustness of these devices must be optimal to ensure their operation in any condition, whether in terrestrial military environments or the vacuum in the space. This implies that designed receivers [20,21] that use robust circuits and redundant systems in the various subsystems, such as the low-noise amplifiers (LNA), high-power amplifiers (HPA), driver amplifier (DA), mixers, combiners, and even filters. Implementing these redundancies and employing durable materials are crucial for reducing the risks associated with potential failures and ensuring the continuity of operations in hostile environments.

In this context, GaN technology emerges as an extremely promising option for developing robust subsystems and circuits [22,23]. Besides its capability to handle high power levels, GaN exhibits a low noise factor, making it a strategic choice for applications in adverse environments such as space and military industries [16,17,24]. The use of gallium nitride (GaN) technology for designing MMICs has grown over the past decade due to its specific properties that make it particularly suitable for designing active RF components [17,24–29]. In comparison to other technologies, like gallium arsenide (GaAs) [30–36], Gallium nitride (GaN), as one of the wide bandgap semiconductors, presents a high electric breakdown field and a high electron saturation velocity. Compared to gallium arsenide (GaAs) and silicon (CMOS or LDMOS) power amplifiers [11,37–41], GaN power amplifiers exhibit higher output power, greater efficiency, wider bandwidth, and better thermal characteristics. Therefore, GaN technology is a strong candidate for high-performance high-power amplifiers [42–47]. Among these characteristics, the most important are the wide bandgap and the high breakdown voltage, which allow MMICs to operate at higher voltages, higher saturation speed, and higher power density compared to conventional GaAs circuits. Additionally, GaN offers excellent thermal conductivity, especially when placed on high-conductivity substrates like silicon carbide (SiC).

Consequently, GaN technology is positioned as a key element for advancement and innovation in these fields, promising to drive the continuous evolution of technological capabilities in space exploration and national defense. In this article, is presented the design of an HPA using 250 nm GaN pHEMT technology from LEONARDO semiconductor's standard GaN pseudomorphic high electron mobility transistor MMIC technology on a substrate thickness of only 100 μm for MFRF systems. Both the output power and the Power Added Efficiency (PAE) are maximized in the frequency band from 2 to 10 GHz at a nominal supply voltage of 28 V.

Additionally, parameters such as bandwidth, large-signal gain, and the compression point not only contributes to the academic understanding of circuit design also has practical implications for real-world applications. This study offers valuable insights for optimizing future circuit designs and improving overall system efficiency. Moreover, the comprehensive nature of the analysis, which encompasses both design considerations and experimental validation, underscores the rigor and validity of the data presented. Through systematic evaluation, this work establishes a solid foundation for future advancements in MMIC technology and contributes to the evolution of high-frequency electronic systems.

In conclusion, this research represents a significant advancement in the field of circuit design and evaluation, demonstrating the successful integration of advanced semiconductor technology

with rigorous experimental validation. This work offers valuable contributions to both academic research and practical applications in the realm of high-frequency electronics. Also accompanied by a comparative analysis between simulations and measurements. This work demonstrates the successful implementation and evaluation of the circuit, and the viability and effectiveness of the chosen approach. Moreover, the utilization of advanced semiconductor technology from [LEONARDO](#) highlights the commitment to leveraging cutting-edge materials and methods in the pursuit of high-performance electronic solutions.

The article is structured as follows. First, the GaN HEMT technology used and its transistor characteristics will be described. Followed by the design and analysis of the proposed HPA. The measured performance of the fabricated amplifier will be provided and discussed before the conclusion.

After the introduction, the main design requirements and objectives are presented in Section 2 under the heading "Issues of Broadband HPA Design." This section includes a series of subsections detailing the initial specifications imposed by [INDRA company](#), the description of the GaN technology used in this project for the design and integration of the HPA MMIC, and the selection of the architecture chosen for the design.

In Section 3, a brief description of the HPA is provided, identifying the main critical aspects. Section 4 presents the measurement setup. For this purpose, the amplifier was assembled in a test bench. The design has been measured "on wafer" and "on jig" and compared with the simulation of the completed design.

Finally, Sections 5 and 6 conclude with a comparison and discussion of the obtained design characteristics and their comparison with the state of the art and other consulted references. The article ends with conclusions about the work carried out and the constructed MMIC.

2. Issues of Broadband HPA Design

2.1. Specifications of Design

Before undertaking any design, the initial specifications for the proposed design must first be presented. Table 1 shows the initial specifications imposed by [INDRA company](#) for the design presented in this article.

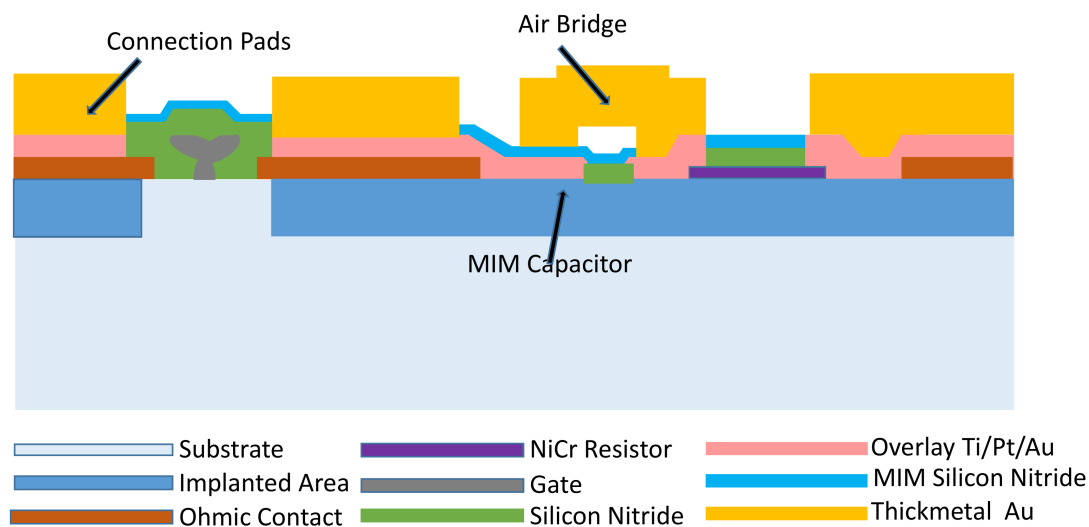
Table 1. Specifications for the HPA

Specification	Value	Units
RF Band, BW_{RF}	2-10	GHz
Stages	≤ 3	NA
P_{OUT}	>42 ($P_{IN}=23$ dBm)	dBm
PAE	>20	%
Large Signal Gain	>19 ($P_{IN}=23$ dBm)	dB
Small Signal Gain	>20	dB
Input Return Loss, IRL	>7	dB
Bias Voltage	>28	V
Size	7.5x7	mm ²
Process&Foundry	GN25 LDO	NA

These specifications (Table 1), as well as the GN25 process from the [LEONARDO](#) GaN foundry, will greatly influence the presented solution, as will be demonstrated in the following sections. As we can see, the initial specifications imposed by [INDRA company](#) are stringent and pose a significant technological challenge that will prove difficult to meet.

Another important aspect to highlight is the large-signal gain specifications, along with the required input power and the number of stages of the HPA, are determined by the application for

The GN25 process is an 0.25 μm gate length and slanted gate-foot profile in AlGaIn/GaN with high electron mobility transistors (HEMT technology) from [LEONARDO](#). The first version of HEMT technology dates back to 2022. In Figure 1, a brief schematic of the GN25 process is shown.



The **LEONARDO** process provides a current gain cut-off frequency $f_T > 22$ GHz, and a maximum oscillation frequency $f_{max} > 44$ GHz. The wafer is thinned in 100 μm . This process is suitable for applications up to 20 GHz with cutting-edge figure of merits in terms of power, gain, and reliability. Table 2 shows the most important characteristics of the MMIC process, provided by the foundry.

L_g (nm)	Thickness (μm)	f_T (GHz)	f_{max} (GHz)	g_{mmax} (mS/mm)	I_{DSmax} (mA/mm)	V_P (V)
250	100	>22	>44	330	950	−3.3 (typ) with $V_{DS}=7\text{ V}$

where:

- L_g is the gate width,
- Thickness is the “thickness of wafer”,
- f_T is the cut-off frequency,
- f_{max} is the maximum frequency at which the transistor can operate as an oscillator,
- g_m is the transconductance,
- I_{DS} is the drain current, and
- V_P is the pinch-off voltage.

Moreover, the MMIC process includes precision Tantalum Nitride resistors (TaN resistors), high values titanium tungstosilicate resistors (TiWSi resistors), Metal-Insulator-Metal capacitors (MIM capacitors), inductors, air-bridges, via-holes through the substrate, CAD models for passive elements and microstrip transmission lines.

It is important to indicate that the GN25 is a process developed for the fabrication of HPAs. Table 3 shows the measured characteristics on wafer at large signal working at room temperature ($T_o=25^{\circ}\text{C}$) in continuous wave (CW) for a transistor of size $10\times100\mu\text{m}$.

Table 3. LDO GN25 Large signal CW $10\times100\mu\text{m}$ transistor performances at $T_a=25^{\circ}$

V_{DS} (V)	I_{DS} (mA/mm)	f_w (GHz)	P_{SAT} (W/mm)	LG (dB)	PAE_{max} (%)
30	150	10	> 6	>16.4	<58
<div>where:<ul style="list-style-type: none">• V_{DS} is the drain to source voltage,• I_{DS} is the drain to source current density,• f_w is working frequency,• P_{SAT} is saturated power density,• LG is the linear gain, and• PAE_{max} is the maximum power-added efficiency.</div>					

The authors of this article used the [LEONARDO's](#) GN25 process because this technology targets the design of monolithic integrated robust high power MMICs besides and by [INDRA company](#) specification.

2.3. Selection of Architecture of the HPA

Based on the data provided by [LEONARDO](#) in the preliminary analysis 2.1, the design specifications 2.2, and taking into account the thermal, electrical, and physical constraints of the technology, a three-stage corporate architecture (2+4+8 transistors) is chosen for the MMIC HPA. Its block diagram is shown in Figure 2, where all transistors in the selected architecture have a size of $10\times100\mu\text{m}$. This transistor choice is due to prior characterization work through Load-Pull simulations using the AWR software version 17 [48]. Although [LEONARDO](#) also provides the PDK for the [ADS](#) [49] software, this variant presents issues when carrying out the final design. Figure 3 shows the Load-Pull analysis for the $10\times100\mu\text{m}$ transistor at frequencies of 2 GHz and 10 GHz, respectively. The figure additionally represents an RC equivalent circuit used to model the output impedance of the transistor.

Once the transistor is selected, the architecture shown in Figure 2 consists of two transistors and four transistors of size $10\times100\mu\text{m}$ for the input and intermediate stages. The final stage is based on the combination of eight $10\times100\mu\text{m}$ transistors in parallel, each providing approximately 33 dBm of output power. This size has been determined taking into account the power density of Leonardo's technology to achieve more than 20 W (43 dBm) at the device's output.

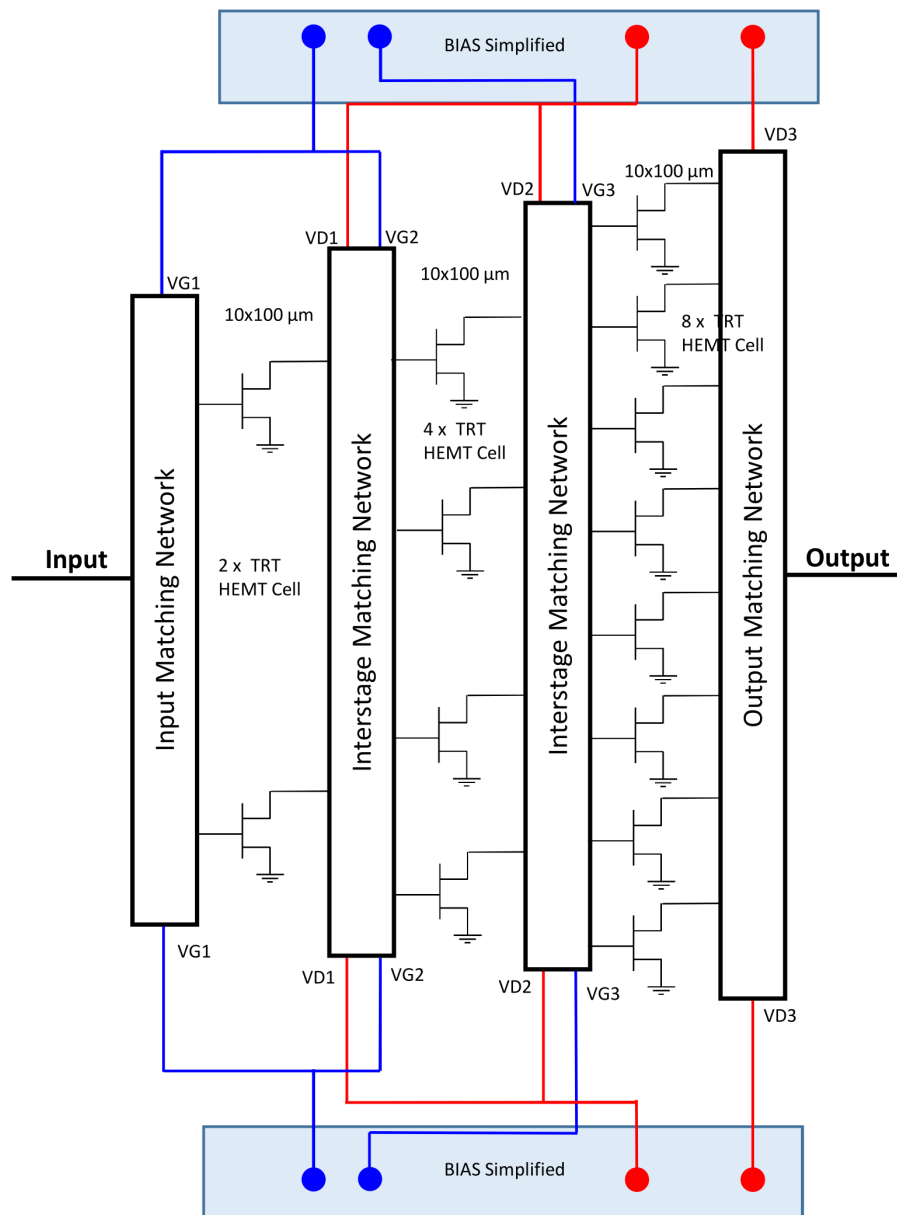


Figure 2. Broadband HPA Architecture.

To simplify the interconnections of the MMIC, the same bias was adopted for all stages, i.e., $V_{DD} = 30\text{ V}$ and $V_{GG} = -3.0\text{ V}$. This corresponds to a quiescent current of 62.5 mA for each device, resulting in currents of 500 mA, 250 mA, and 125 mA in the final, intermediate, and input stages of the HPA, respectively. This choice is the result of a compromise between electrical performance and the capabilities provided by the [LEONARDO](#) PDK.

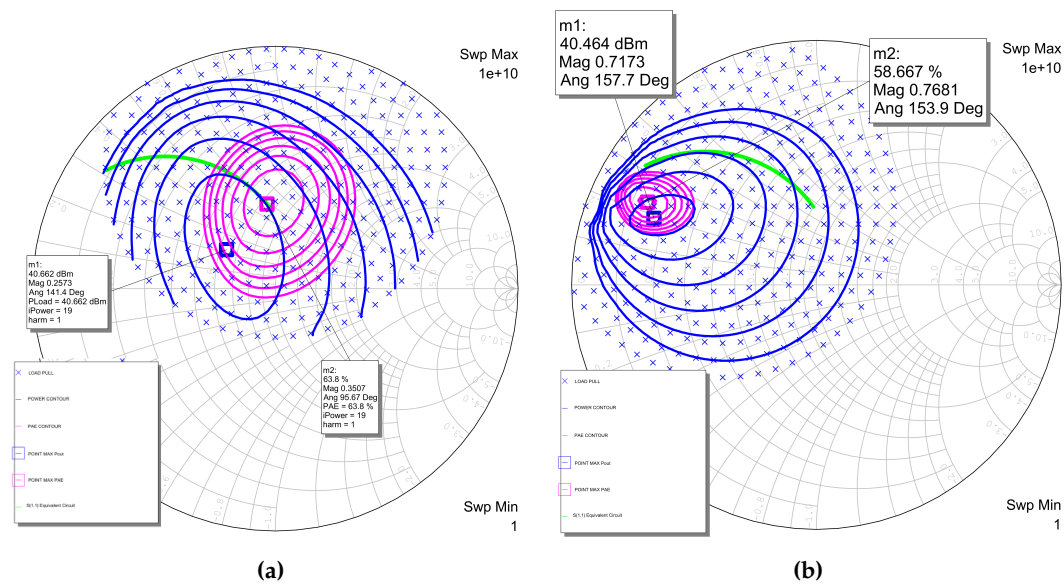


Figure 3. Load-Pull Characterization of the 10x100 μm Transistor. Analysis at 2 GHz [3a](#)) and 10 GHz [3b](#))

3. Hpa Networks Strategy, Simulations and Design

Once the architecture was established and the transistors were selected, the next step was to concisely describe the strategy followed in the design. The authors have described the steps taken and the strategy employed in the design of the HPA MMICs in greater detail in the article [50].

The optimal operating class depends on the application area. This high-power amplifier discussed in this work is designed for applications in EW. Therefore, the most important requirements are both output power and added power efficiency (PAE) simultaneously. Hence, class-AB is the best choice to achieve these requirements. In this design, all stages have been biased in class-AB to ensure PAE performance. This biasing point which guarantees accurate nonlinear simulation.

As described in [50], the synthesis of input and output impedances to maximize output power and PAE for each stage, along with the power distribution and combining networks, constitute the essential aspects of simulating the HPA MMIC design [51,52]. In a design for wide bandwidth, harmonics are of little importance and are matched to 50 ohms. The design of impedance matching networks and power distribution/combining networks was initially approached using the equivalent circuit extracted from the Load-Pull, as described in [50].

In Figure 4, the test bench in AWR is shown for calculating all the required specifications mentioned in Section 2.1.

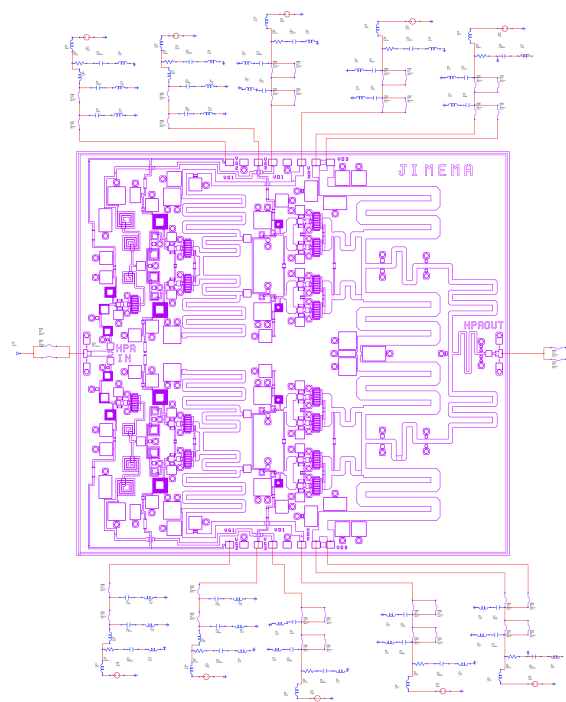


Figure 4. AWR Setup for Broadband HPA Characterization

In the final design, the transmission lines and connection lines modeled by the Leonardo PDK with real lines are simulated by the EM simulator. This is due to the proximity and bandwidth of the specified frequencies. Therefore electromagnetic simulation is employed with the assistance of AXIEM of AWR. In Figure 5, a schematic of the designed HPA is shown, illustrating the complexity of the design and the various networks comprising it.

The AXIEM electromagnetic tool from AWR software allowed us to assess the effect that lines and passive elements have on the final behavior of the designed broadband HPA. In the simulations carried out, the circuit model for the lines and passive elements, provided by the LEONARDO foundry, and the electromagnetic model that the ADS software allows modeling were studied.

Figure 6a and 6b display the results of the small-signal and large-signal parameters of the final designed MMIC. As we can be observed, these simulations enable the prediction of meeting the initial requirements.

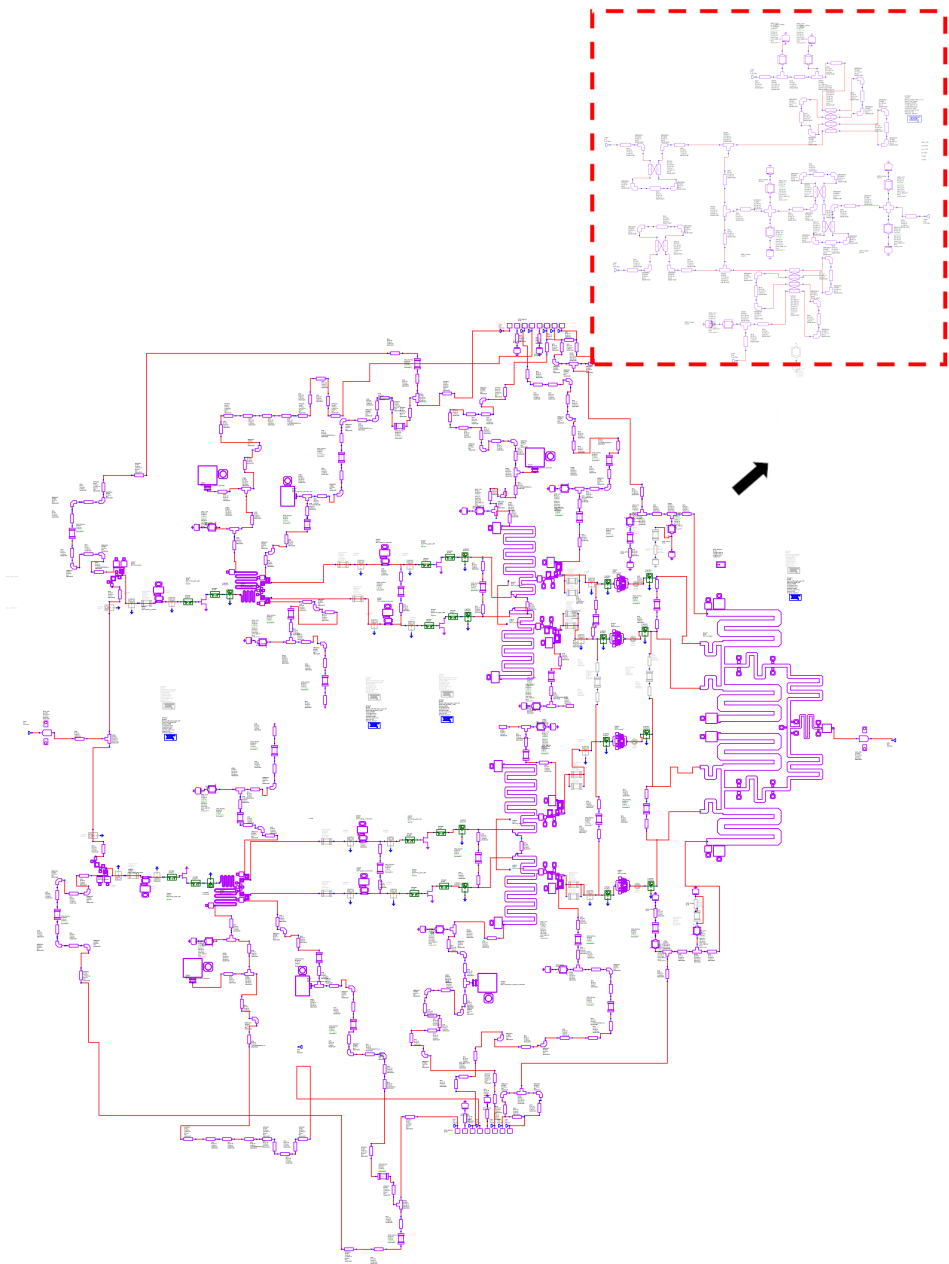


Figure 5. Electric Scheme of the Broadband HPA

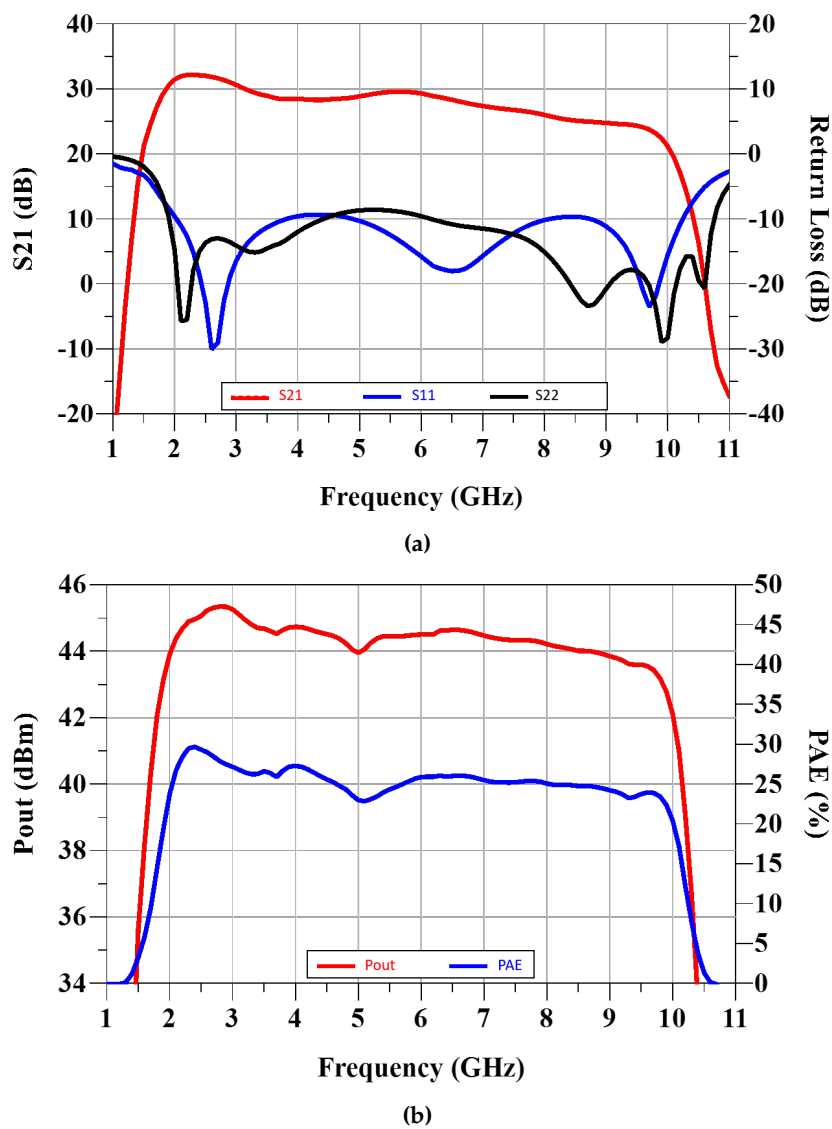


Figure 6. EM Simulations. Small Signal 6a) and Large Signal 6b)

After this performance verification, the HPA MMIC is fabricated at the [LEONARDO Foundry](#). Figure 7 shows a photomicrograph of the constructed HPA MMIC.

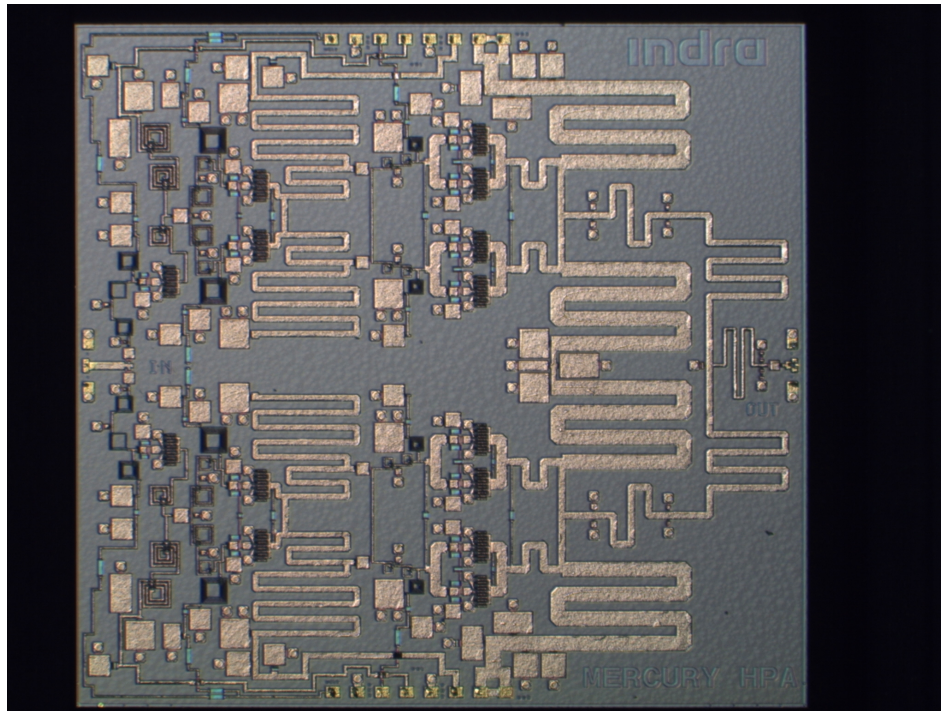


Figure 7. Microphotograph of the fabricated MMIC (chip size is 7.5 mm x 7 mm)

3.1. Stability Analysis

Theoretically, the analysis of any stability criteria [53,54] can be usefully applied to verify the unconditional stability of the two-port network in the small-signal regime. Unfortunately, as described in numerous articles [50,55,56], a high-frequency HPA (power amplifier) cannot be adequately modeled as a two-port network. This is because an HPA MMIC has a complex structure with multiple bias ports and paths for the RF signal. This leads to, as predicted by Platzer [55], oscillations or instabilities that cannot be adequately detected solely with the k-stability test from the small-signal S-parameters of two-port networks. This requirement is necessary but not sufficient because compliance with it does not guarantee circuit stability. It is well known [53–56] that if the final circuit simulation results in a circuit that meets the classical stability condition, then the μ factor [54] obtained will be greater than 1 in the amplifier's operating frequency band, but it does not assure the instabilities of the internal feedback paths.

To ensure the stability of the designed HPA MMIC, in this case a stability criterion in LS (large-signal) is applied, identifying pole-zero locations at various nodes of the HPA MMIC and for different power levels. Therefore, to guarantee the unconditional stability of the amplifier and ensure that no instabilities appear, stability analyses are conducted in both small and large signal domains, as shown in Figure 8.

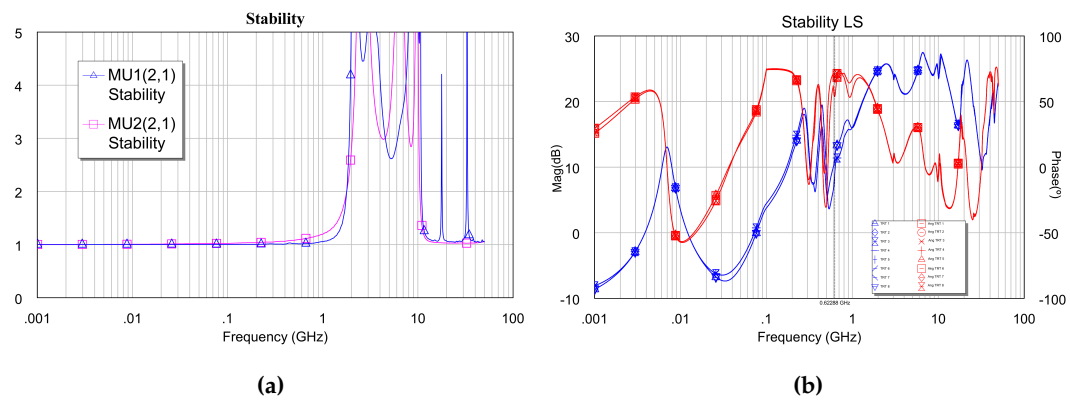


Figure 8. Stability Analysis. Small Signal 8a) and Large Signal 8b)

4. HPA Measurement

In this section, the results obtained from the measurements are presented and compared with the simulations conducted in AWR for the designed HPA MMIC. "On-wafer" measurements of the HPA have been carried out by the LEONARDO Foundry. The article shows the two sets of measurements conducted "On Wafer" and "On jig". For the "On jig" measurement, the HPA MMIC has been mounted on a carrier by [INDRA company](#), as shown in the photograph in Figure 9.

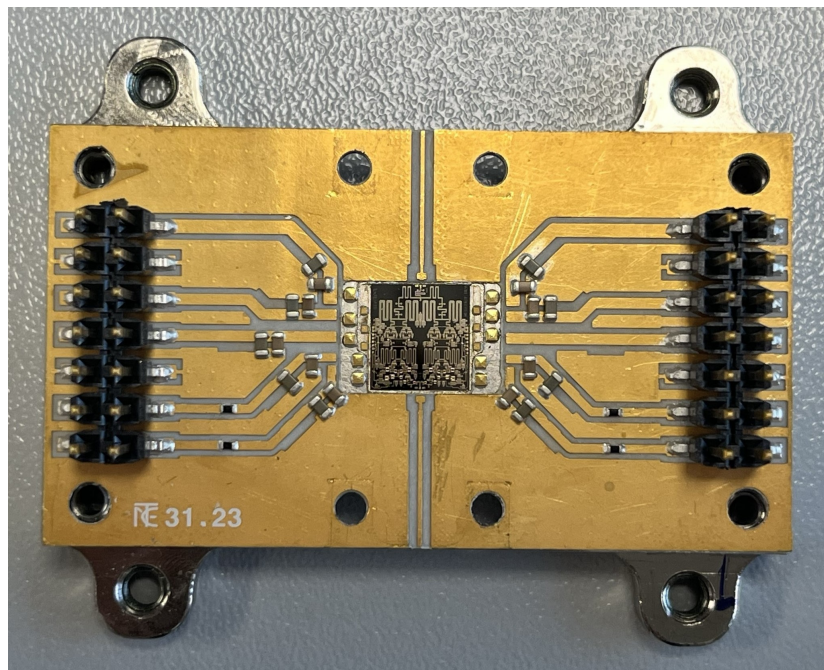


Figure 9. Photograph of the MMIC "on jig" (size is 42.5 mm x 31.5 mm)

The HPA MMIC was mounted for "On jig" measurements on a board specifically designed for measuring these circuits. This board was constructed on a Rogers 3003 substrate ($\epsilon_r = 2.2$, $h = 5$ mil) from Rogers Corporation. The input and output connectors chosen were ELF-KN 2.92 mm Edge Launch connectors from Southwest Microwave. Once the circuit was mounted on the board, interconnections between the MMIC and the board were made using wire bondings. The MMIC bonding wires have a length close to $160 \mu\text{m}$ at the inputs and outputs, with a diameter of $25.4 \mu\text{m}$. The distance between the chip's input/output line and the board is approximately $70 \mu\text{m}$.

Next, once mounted as previously mentioned, the circuit is characterized and measured. The circuit assembly is arranged according to the layout shown in Figure 10a. Figure 10b shows the instruments used in the measurement setup.

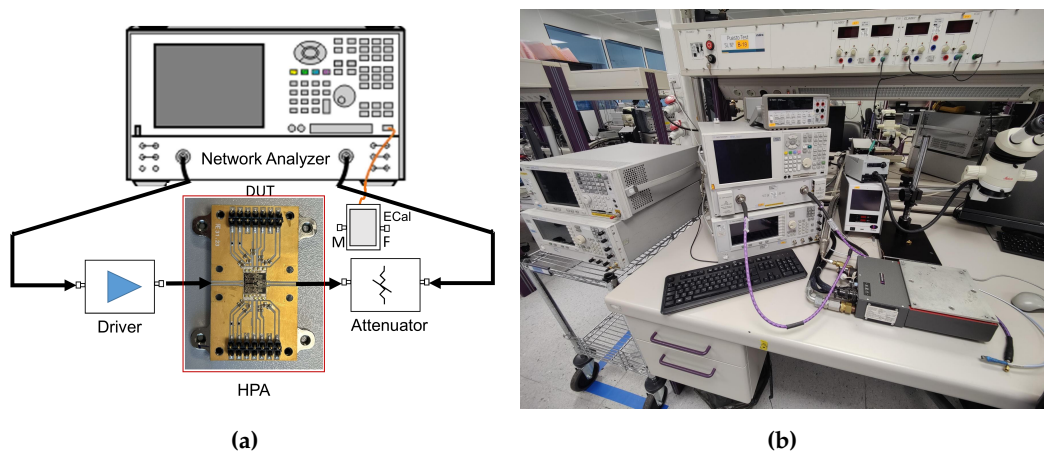


Figure 10. Scheme of the test bench small and large signal “on jig”. Core jig 10a) and test bench 10b)

For better clarity, the measurements conducted are presented in two subsections, corresponding to small-signal measurements and large-signal measurements.

4.1. Small-Signal Measurements

Firstly, although small-signal measurements are less important for power amplifiers compared to other circuits such as low-noise amplifiers (LNAs) or drivers, they were conducted to verify the accuracy of the design. The S-parameters were measured using the Keysight PNA-X vector network analyzer with electronic calibration. The return loss values at the input and output are greater than 11 dB, $|S_{11}|^2 > 7$ dB, and $|S_{22}|^2 > 5$ dB. These values indicate an acceptable level in the port matching for the input and output of the HPA. Additionally, as observed in the Figure 11, there is excellent agreement between the simulation and the measured results.

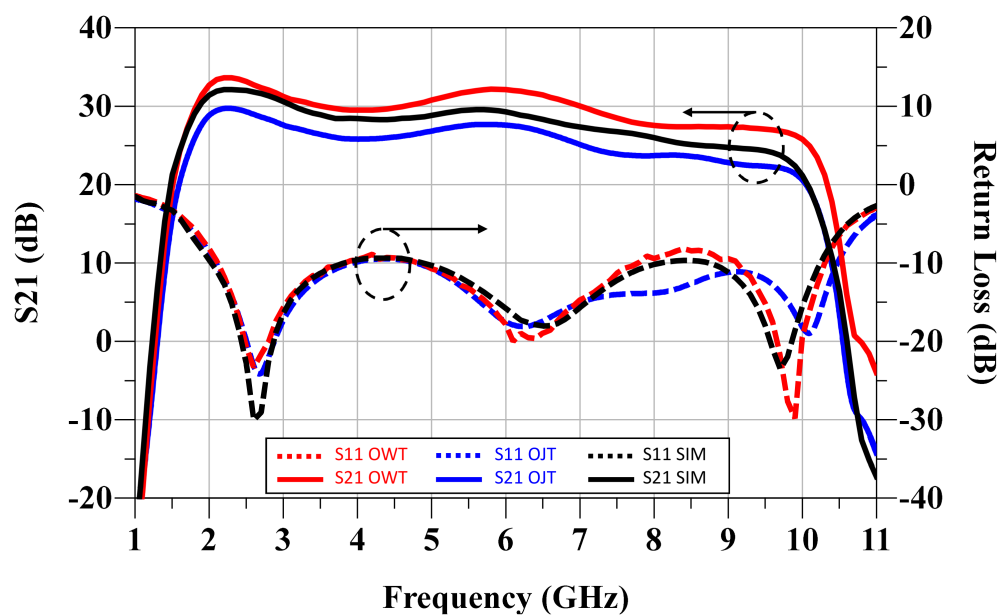


Figure 11. Small Signal Measurements.

However, as previously mentioned, these values lack the importance they hold for other RF/MW devices. Let's recall the fundamental role and function of an HPA, which is to operate in large-signal conditions. This implies that the amplifiers function in a nonlinear regime where the assessment of return losses is not as critical.

The small-signal measurement of the HPA was completed via Keysight vector network analyzer (VNA) N5242 B (Keysight Technologies, Santa Rosa, CA, USA). Figure 8 demonstrates the measured S-parameters in comparison to the simulated ones. It is evident that the measurements and simulations are in good consistency. The amplifier achieves a small-signal gain of 24–25.5 dB with gain flatness less than ± 0.75 dB across the frequency range of 2–6 GHz. The measured input and output return losses are better than 14.5 and 10 dB, respectively, achieving good input and output matching

4.2. Large-Signal Measurements

RF and microwave HPAs play a crucial role in the output stages of RF and microwave chains in both communication systems and electronic warfare. One of the measurements that truly characterize the HPA correspond to large-signal measurements. To optimize system performance, it is important to understand its key performance metrics are P_{OUT} and PAE , as primary parameters.

In summary, understanding and optimizing P_{OUT} and PAE are essential for the efficient and effective design of RF and microwave amplifiers in a wide range of applications.

- **Performance Evaluation:** These metrics provide a direct assessment of the amplifier's performance in terms of the amount of output power it can deliver and the efficiency with which it converts input power into output power
- **Energy Efficiency:** PAE is especially important as it indicates how much input energy is effectively converted into useful output energy. High energy efficiency is crucial for minimizing power consumption and maximizing battery life.
- **Design and Optimization:** Understanding these metrics is essential for designing and optimizing RF and microwave systems. It allows engineers to make informed decisions about component selection, circuit topologies, and biasing strategies to achieve desired performance levels.
- **Impact on Signal Quality:** P_{OUT} and PAE can also impact the quality of the output signal. High output power can improve transmission capacity and signal coverage, while high efficiency can reduce distortion and improve signal fidelity

As previously mentioned, measurements performed both “On wafer” and “On jig” are presented, along with their comparison with the simulated results. For the measurements, the test bench and instrumentation shown in Figure 10 have been used. Besides, as explained before, the jig structure has parasitic effects that cannot be de-embedded and, added to the thermal effect of the CW excitation, makes the gain on the jig lower than the simulated or the OW ones.

The large-signal measurement was measured using Vector Network analyzer (VNA) N5242 B Keysight (Keysight Technologies, Santa Rosa, CA, USA), drive amplifier, and attenuator. A under driving CW signal. The measured saturated output power (P_{out}), PAE , and gain against frequency are demonstrated in Figure 12. In this case, the input power (P_{in}) is fixed as 23 dBm. The output power varies from 45.7 to 43 dBm, and PAE are within 30–20%, respectively. The lack of power in the on-jig measurements in comparison with the on-wafer measurements can be explained due to the thermal effect.

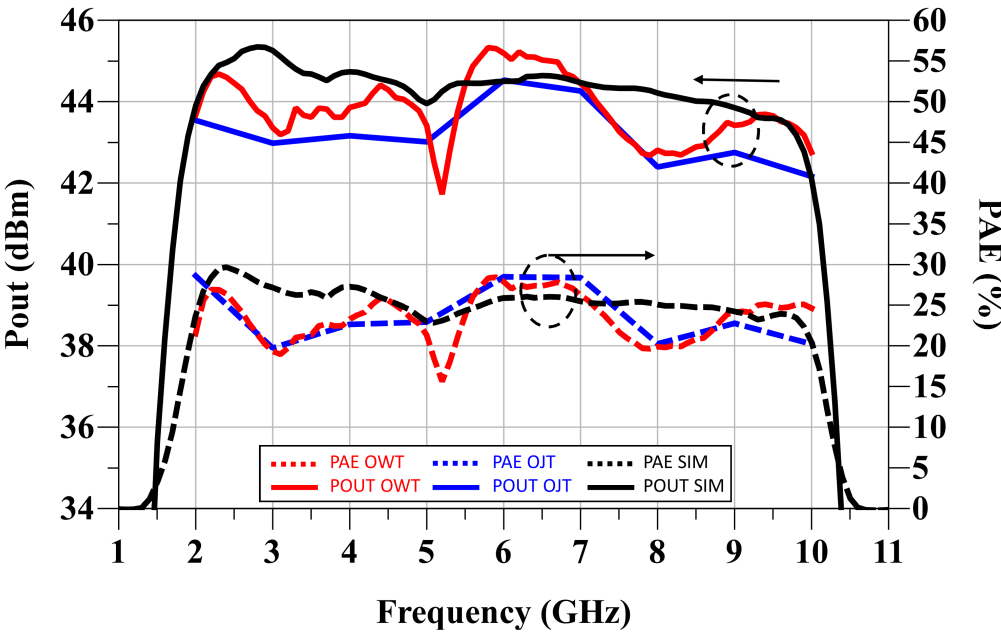


Figure 12. Large Signal Measurements ($P_{IN}=23$ dBm).

The Figure 13 shows the measurement of the current consumed by the MMIC with an input power of 23 dBm. It can be observed that there is great agreement between the simulation and the measurements.

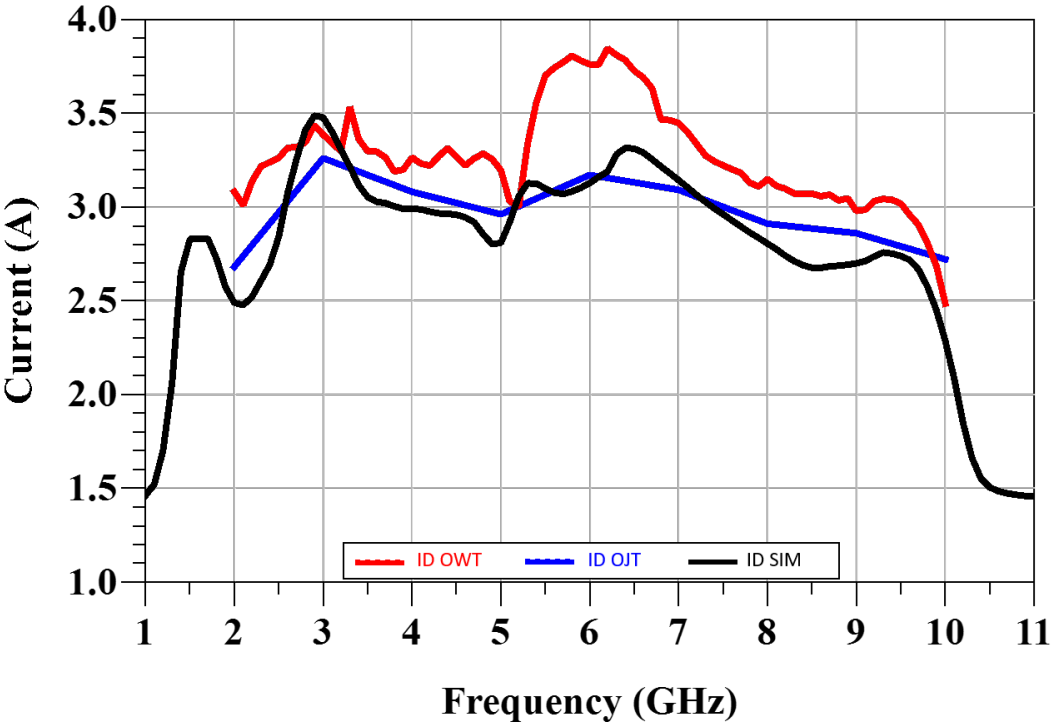


Figure 13. Current Measurements ($P_{IN}=23$ dBm).

4.3. Sumary of Performances

After conducting small and Large Signal measurements, the results are presented in Table 4, where we can compare and observe the compliance with almost all design specifications, with the

exception of IRL, which is slightly lower. However, the MMIC is still valid as HPA suitable as a first approximation to the initial specifications.

Table 4. Compliance Table the MMICs Mixer manufactured in this research.

Specification	target	HPA	Units	Compliance
RF Band, BW_{RF}	2-10	2-10	GHz	C
Stages	≤ 3	3	NA	C
P_{OUT}	>42 ($P_{IN}=23$ dBm)	>43 ($P_{IN}=23$ dBm)	dBm	C
PAE	>20	>20	%	C
Large Signal Gain	>19 ($P_{IN}=23$ dBm)	>19 ($P_{IN}=23$ dBm)	dB	C
Small Signal Gain	>20	>20	dB	C
Input Return Loss, IRL	>7	>7	dB	PC
Bias Voltage	>28	>28	V	C
Size	7.5×7	7.5×7	mm^2	C
Process&Foundry	GN25 LDO	GN25 LDO	NA	C

where: C=Compliance PC = Partially Compliance. NC = Non Compliance

5. Discussion

Table 5 shows a comparison of the performance of the designed HPA with other published MMIC HPAs in similar frequency bands to the specified requirements. In recent years, to meet the high demand for broadband work and increased performance in applications below 20 GHz, high-efficiency broadband amplifiers have been extensively studied. They have been compared with various amplifiers starting with GaAs technology [33], where its lower power level compared to GaN technology is evident. Next, it has been compared with various GaN HPAs with higher broadband power levels manufactured to cover similar frequency and power ranges as specified, maintaining output power levels in the order of watts. In [45], a non-uniformly distributed GaN power amplifier from 0.5 to 6.5 GHz was presented with a small chip area to achieve output power greater than 30 dBm and a PAE of 20-38.1%. In [46], a GaN power amplifier from 2.5 to 10.5 GHz was implemented with distributed amplifier stages at the input and a reactively tuned corporate stage at the output to achieve saturated output power of 18–37 W and a PAE of 19–40%. In [47], an interesting work is shown, where an HPA MMIC covering the 2 to 6 GHz band and an output power of 10 watts with a PAE value exceeding 35%.

Finally, the designed HPA MMIC has been compared with a commercial GaN power amplifier from Qorvo [57] with relatively similar performance. It is worth noting that although the proposed design has a larger size than the referenced ones, this is largely due to the output power value. Regarding gain and PAE, it should be noted that the value is in line with the current state-of-the-art and as of the date of this article.

The obtained results demonstrate that the performance of the HPA is satisfactory compared with the performance of other HPA reported in the literature on this topic. Table 5 shows a comparison of the proposal of this article with five very good proposals that can be considered references in the field of HPA design.

Table 5. Performance Comparison of the HPA MMICs

Parameter	This Work	[33]	[45]	[46]	[47]	[57]
Process	250 nm GaN	150 nm GaAs	500 nm GaN	250 nm GaN	250 nm GaN	150 nm GaN
Stages	3	2	3	2	2	2
Architecture	C	C	D	D(I)+C(O)	C	C
Frequency (GHz)	2-10	2-6.5	0.5-6.5	2.5-10	2-6	1-8
IRL (dB)	> 9	> 9.5	> 10	5-20	14.5	13.2-14.4
ORL (dB)	> 7.5	NR	> 7	5-10	>10	16.7-21
P_{out} (dBm)	43.0-45.7	31-32	30-33.5	42.5-45.7	44.4-45.2	39.4-40
PAE (dB)	22.7-43.0	31.4-51.5	20-38.1	19-40	35.8-51.3	30.4-46.8
DC supply (V)	30	5	15	40	28	28
Current supply (A)	3.1 (max)	NR	0.330 (I_{DQ})	NR	1.2 (I_{DQ})	0.65 (I_{DQ})
Stability	OK	NR	NR	NR	NR	NR
Chip Size (mm x mm)	7.5 x 7	3.7 x 2.6	2.0 x 2.0	5 x 4	3.5 x 4.1	3.3 x 3.55

where: NR = Not Reported. C=Corporate. D=Distributed. (I)=Input. (O)=Output

6. Conclusion

A high-power amplifier has been designed and measured in the 2 to 10 GHz frequency band for MFRF systems using Leonardo’s 250 nm GaN technology process (LDO GN25). This amplifier represents a significant advancement in communication and radar system development, offering an efficient and powerful solution for multifunctional applications.

The meticulous design and precise implementation of GaN technology allow the amplifier to achieve more than 43 dBm of output power, setting a new standard in terms of performance and transmission capability. Additionally, the power added efficiency exceeds 20 %, ensuring cost-effective and environmentally friendly operation.

In terms of power consumption, the MMIC exhibits a drain current consumption of less than 4 A across the frequency band, making it highly energy-efficient. Detailed characterization of the amplifier reveals excellent agreement between theoretical simulations and measurements, validating the accuracy and reliability of the design.

During on-wafer measurements, even higher gain is observed than predicted by simulations, suggesting even greater potential for this amplifier under real operating conditions. However, large signal results show slightly lower output power than simulations, which may be attributed to a thermal effect due to heat generated during operation.

In summary, this HPA represents an ideal option for integration into future TRMs for AESA systems. Its ability to deliver high levels of output power, energy efficiency, and reliability makes it a versatile and adaptable solution for a wide range of applications, including radar, electronic warfare, and communications, all within the same system.

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J.M.-P.; supervision: A.F.-E., V.G.-P and E.O.-G.; chip acquisition: A.F.-E., A.P.-P and J.M.-P; measurements: A.F.-E., A.P.-P and E.O.-G. All authors have read and agreed to the published version of the manuscript. Authorship was limited to those who contributed substantially to the work reported

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