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Article

DC Solid-State Circuit Breakers with Two-Winding Coupled Inductor for DC microgrid

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Abstract: Ensuring a protection scheme in DC distribution is more difficult to achieve against pole-to-ground fault than in AC distribution system because of the absence of zero crossing points and low line impedance. To complement the major obstacle of limiting the fault current, several compositions have been proposed related to mechanical switching and solid-state switching. Among them, solid-state circuit breakers(SSCBs) are considered a possible solution to limit fast fault current. However, they may cause problems in circuit complexity, reliability and cost-related troubles due to the use of multiple power semiconductor devices and additional circuit configuration to commutate current. This paper proposes the SSCB with a coupled inductor(SSCB-CI) which has symmetrical configuration. The circuit is comprised of passive components like commutation capacitors, a CI and damping resistors. Thus, proposed SSCB-CI offers the advantages of simple circuit configuration and fewer utilized power semiconductor devices than another typical SSCBs in LVDC microgrid. For analysis, six operation states are described for the voltage across main switches and fault current. The effectiveness of the SSCB-CI against a short-circuit fault is proved via simulation and experimental results in a lab-scale prototype.

Keywords: Solid-state DC circuit breaker; Coupled inductor; Pole-to-ground fault protection; LVDC(Low voltage DC) microgrid protection.

1. Introduction

In recent years, DC power systems have come to the fore in microgrid and distribution systems configuring DC-based renewable energy such as PV and battery charging station[1],[2]. These features have prompted DC applications in shipboards, airplanes, telecommunication systems, and data centers[3]-[5]. However, fault detection and isolation to a fault area are still major technical barriers of DC-based system. In a distribution network, fault protection against short circuit has difficulties. In AC distribution, the fault current is limited by high line impedance at commercial frequency with zero crossing points. However, in DC distribution, the absence of zero crossing points and lower line impedances compared with AC distribution lead to a high fault current magnitude under pole-to-ground short-circuit fault[6]. Moreover, the fault current has become an important issue in energy storage systems, which has motivated steady research into this area[7],[8]. So far, some challenges have arisen for limiting the fault current and reducing the clearing time on the fault area. In order to ensure protection against fault accidents, mechanical CB and solid-state CB are considered principally. Mechanical CB has the advantages of lower conduction loss, but it has a breaking time of about several tens of milli seconds[9],[10]. Thus, the solid-state circuit breakers (SSCBs) with fast response time have become a solution for the quick isolation of a fault section.

SSCBs have been proposed in many studies to verify the validity of fault isolation effectively, and they have mainly dealt with the requirements of fast fault clearing time or noticeable circuit configuration using several kinds of power semiconductor device. In

order to achieve affordable circuit configuration and beneficial effects, the principally considered methods are circuit configuration based on power semiconductor devices or artificially commutating the fault current [11]-[12].

In [11], SCR-based SSCBs have been proposed with the main goal of reducing the number of inductors compared with the bi-directional SSCB in [12]. A three-winding transformer is adopted with a number of power semiconductor devices, two thyristors and two diodes. However, in this circuit configuration, complex circuit configuration is caused by several components. Moreover, proposed method needs an external circuit to commutate SCRs. Therefore, SCR-based SSCB still has a limitation in the aspect of simple circuit configuration.

Another solution with SSCB based on silicon carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFETs) has been proposed[13]. Si power devices have some notable advantages compared with SCR in terms of superior material properties such as thermal conductivity, energy gap and conduction losses. However, SiC-based SSCB is not cost-effective so far. Therefore, a circuit configuration with SiC may increase the circuit cost.

As another way to insert a commutation path with passive components, LC resonance circuits are considered[14],[15]. LC resonance is a basic solution to create zero crossing points, and is one solution to limit or cut off the fault current. In these studies, a capacitor and an inductor are inserted in series to transform the fault current path into LC circuit, so that the DC current wave can be changed into a sine wave passing by zero crossing points. However, one drawback is the need for an additional circuit to pre-charge commutation capacitor, which increases the complexity of the circuit configuration of SSCB. Also, the increased number of inductors causes an increase in the volume of the overall topology. In a way to insert inductance into the circuit, a coupled inductor(CI) is considered. The CI is a solution in the optimization of two or more inductors by one magnetic component[16],[17]. Therefore, it has the advantage of simple configuration with bi-directional energy flow and fault interruption[18]-[20].

This paper presents a novel DC SSCB circuit without additional power semiconductor devices except for a main switch that complements the aforementioned problems. With the traditional circuit configuration in SSCBs, the reported topologies rely on multiple power semiconductor devices that are employed to block an instantaneous short circuit current and a voltage spike. To come up with effective method about drawbacks due to the complex circuit configuration and cost-related problem, several passive components, capacitors, resistors and two-winding coupled-inductor, are employed without semiconductor devices. The circuit configuration is combined based on the basic idea of series LC resonance and damping resistors. Capacitors are inserted to generate alternate commutating current in short circuit fault. Detailed explanation of operation states and circuit configuration is presented in Section 2. Section 3 and 4 illustrate results about simulated fault interruption in a lab-scale prototype. In the end, conclusion and necessary improvements of SSCB-CI are discussed in Section 5.

2. Operation of the SSCB-CI

The circuit configuration of the SSCB-CI is illustrated in Fig. 1, where the overall current flow and across voltages are denoted. The proposed circuit is functionally divided into several parts. Except for main switches SW_{main}, power semiconductor devices to block the fault current are not needed. The two-winding CI is given to commutate the sinusoidal current through zero crossing points from fault section to the secondary winding. Also, the CI is utilized to insert the commutation path in each windings. The inserted capacitors, C_{pri} and C_{sec}, generate the sinusoidal currents. The main function of the series resistances, R_{seri_p} and R_{seri_s}, are to damp the transient oscillation of the fault current and to limit the magnitude of the current to charge C_{pri} and C_{sec}. The parallel resistors, R_{para_p} and R_{para_s} are linked to block an instantaneous voltage spike of the winding voltages, V_{pri} and V_{sec}.

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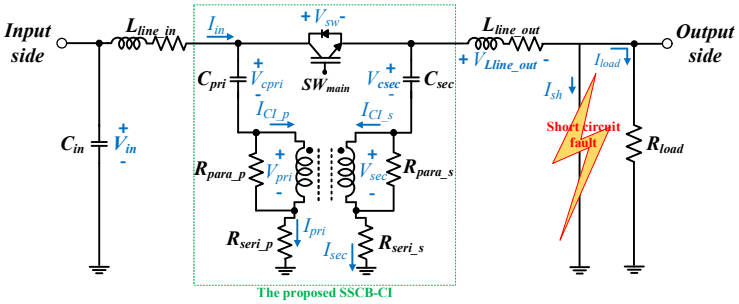

Figure 1. Circuit configuration of the proposed SSCB-CI.

The proposed circuit configuration with symmetrical structure has the advantage of responding to a short-circuit fault on both the input side and the load side[21]. Designing a CI is an important issue. A self-inductance can be designed by a turns-ratio, and leakage inductance can be designed by a coupling coefficient, *k*. Previous studies on the use of a two-winding CI have confirmed that the higher the value of k, the better the dynamic response of the inductor current[22]. Thus, a *k* having high value is also considered in proposed circuit configuration. Overall operation states of the SSCB-CI are shown in Fig. 2. In this figure, each state from state 1 to 3 represents the current flow when the circuit breaker is initially operated in the steady state of the DC microgrid. From state 4 to 6, these states represent the current flow under the pole-to-ground fault of load side. The key waveforms in each parts about overall operation states are shown in Fig. 3. Detailed explanations depending on each state are as follows:

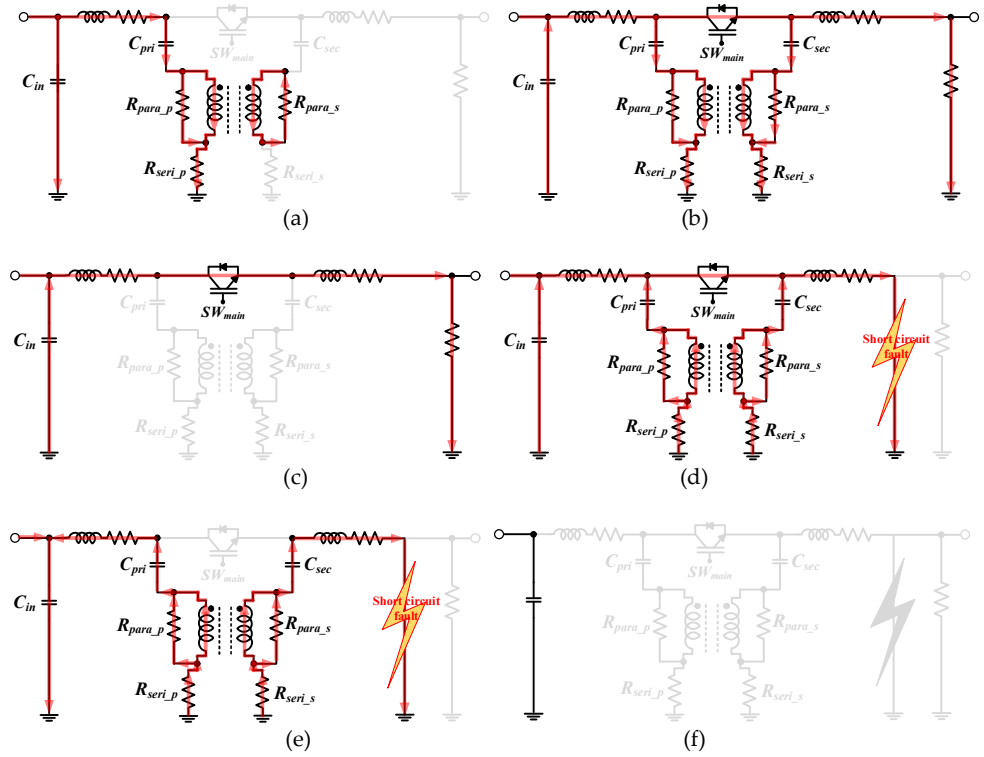

Figure 2. Operation states of SSCB-CI: (a) State 1: Pre-charge of primary winding capacitor. (b) State 2: Pre-charge of secondary winding capacitor. (c) State 3: stationary. (d) State 4: Time interval. (e) State 5: Block and commutation. (f) State 6: Protection.

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ⅰ. State 1: Pre-charge of commutation capacitor in the primary side(t_0~t_1)

This state is occurred to charge C_{pri} under steady state of DC microgrid. In Fig. 2 (a), this state means initial state of the SSCB-CI, and occurs when SW_{main} turns off at normality of input voltage V_{in}. During this state, C_{pri} is charged. The initial condition of I_{sh}, I_{pri} and I_{in} can be expressed as (1).

$$I_{sh} = 0,\ I_{pri} = 0,\ I_{sec} = 0\ and\ \frac{di_{in}}{dt} = 0 \tag{1}$$

The voltages across capacitors, V_{Cpri} is similar to V_{in}. After charging, the primary winding current I_{CI_P} is removed, thereby eliminating unexpected power losses by R_{para_p} and R_{seri_p} in the stationary state.

ii. State 2: Pre-charge of commutation capacitor in the secondary side (t_1~t_2)

After State 1, if SW_{main} turns on, C_{sec} is charged, and it can be shown as Fig. 2 (b). The current flow in the secondary winding is similar as in State 1, but C_{pri} is discharged temporarily because of voltage fluctuation of secondary winding voltage V_{pri}. After that, C_{pri} is charged again as V_{in}, where, the input current and the input voltage can be expressed respectively as (2) and (3).

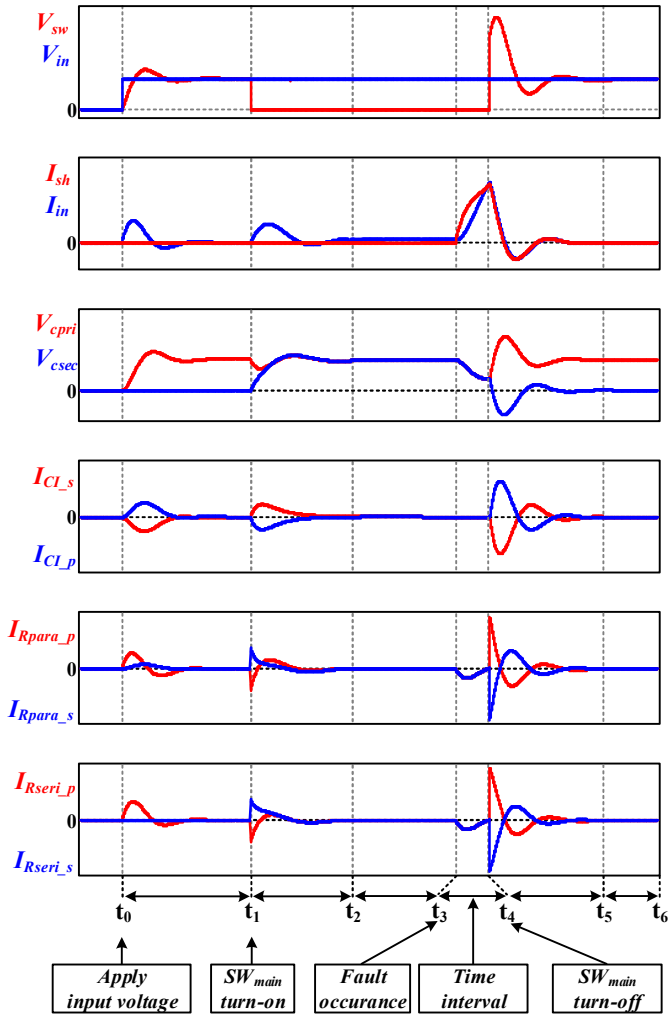

Figure 3. Key waveforms of the SSCB-CI under operation states

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$$i_{in} = i_{pri} + i_{sec} + i_{out} = i_{pri} + i_{sec} + i_{sh} + i_{load} \tag{2}$$

$$v_{in} = \frac{1}{C_{pri}} \int i_{pri} \cdot dt + v_{Cpri}(t_1) - k v_{\sec} + \left(1 - k^2\right) L \frac{di_{CI\_p}}{dt} + R_{seri\_p} i_{pri} \tag{3}$$

Where, L is the self-inductance of each winding, L_p and L_s, where two self-inductances are considered herein to have equal inductance. That is, the CI is modeled as an ideal transformer, which has a turns ratio of 1:1, same magnetizing inductor, and same leakage inductor. Also, the winding resistance is neglected for ease of understanding. Therefore,

$$L_p = L_s = L \tag{4}$$

iii. State 3: Stationary(t_2~t_3)

This state means the interval between capacitor charging state and time interval state, as shown in Fig. 2 (c). SW_{main} is continuously turned on and input current I_{in} flows to the load as I_{load}.

$$I_{in} \approx I_{load} \tag{5}$$

Until line-to-ground short-circuit fault, the SSCB-CI stays. At this state, I_{CP_P} and I_{CP_S} are removed as zero. Also, the voltages across C_{pri} and C_{sec} are regarded as equal to V_{in}.

iv. State 4: Time interval(t_3~t_4)

Fig. 2 (d) indicates the voltage and current rise after the line-to-ground fault. In this state, the instantaneous fault current is generated because of the short-circuit fault at the load side. However, SW_{main} is not turned off immediately because of the short interval time by trip delay and fault detection. Therefore, I_{in} and I_{sh} are increased simultaneously. During this state, I_{sh} can be expressed as (6). In this equation, only inductance, L_{line_in} and L_{line_out} as line impedance are considered for easy analysis.

$$i_{sh}(t_4) \approx \frac{1}{L_{line\_in} + L_{line\_out}} \int \left\{ v_{in} - \left(R_{line\_in} + R_{line\_out} \right) i_{in} \right\} dt + i_{Load}(t_3) \quad where,\ i_{Load}(t_3) \approx 0 \tag{6}$$

Where, R_{line_in} and R_{ine_out} mean resistor components of each line impedance.

V. State 5: Block and commutating fault current(t_4~t_5)

Fig. 2 (e) shows the commutating fault current flow. When the detected level of I_{in} is exceeded this state occurs, and consequently SW_{main} is turned off. Fault current in State 5 can be assumed as (7).

$$i_{sh}(t_{state5}) = \frac{V_{in}}{L_{line\_out}\omega_d} e^{-\alpha t} \sin \omega_d t + i_{sh}(t_4) \quad where,\ \omega_d = \frac{\sqrt{4L_{line\_out}C_{\sec} - \left\{ (R_{para\_s} + R_{seri\_s}) C_{\sec} \right\}^2}}{2L_{line\_out}C} \tag{7}$$

Where, α and ω_d mean respectively the damping ratio and the resonant frequency by L_{line_out} and C_{sec}. Consequentially, the larger the resistance value, the larger the damping ratio.

After I_{sh} reaches the peak level, SW_{main} is stressed to more than V_{in}, namely a blocking voltage. Where, V_{sw} at state 5 can be expressed as follow.

$$V_{L\_line\_out}(t_{state5}) = \frac{V_{in}}{\omega_d} e^{-\alpha t} \left(-\alpha \sin \omega_d t + \omega_d \cos \omega_d t \right) \quad Where,\ \alpha = \frac{R_{para\_s} + R_{seri\_s}}{2L_{line\_out}} \tag{8}$$

$$V_{sw}\left(t_{state5}\right)=V_{in}-V_{L\_line\_out}\left(t\right)=V_{in}\left\{1-\frac{1}{\omega_d}e^{-\alpha t}\left(-\alpha\sin\omega_d t+\omega_d\cos\omega_d t\right)\right\} \quad (9)$$

After I_{sh} reaches the peak level, SW_{main} is stressed as V_{SW_max}, namely a blocking voltage as (10) and (11).

$$t_{\max}=\frac{1}{\omega_d}\arctan\left(\frac{2\alpha}{\frac{\alpha^2}{\omega_d}-\omega_d}\right)+\frac{\pi}{\omega_d} \quad (10)$$

$$V_{SW\_\max}=V_{SW}\left(t_{\max}\right) \quad (11)$$

After I_{sh} reaches the peak level, SW_{main} is stressed as V_{SW_max}, namely a blocking voltage. During this state, I_{sh} flows through the secondary winding by discharging the capacitor energy of C_{pri} and C_{sec}. As C_{sec} discharges, V_{Cpri} and V_{Csec} oscillate momentary for a few micro seconds, and then become stable. As a result, an induced energy to the primary winding decreases Ish. Due to the series resonance configuration, the current waveforms in the SSCB-CI circuit are produced as a sinusoidal current which has zero crossing points, and is damped by R_{seri_p} and R_{seri_s}.

VI. State 6: Protection (t_5~t_6)

The final state is the isolation of the load to V_{in} after a short-circuit fault. After blocking the fault current, C_{sec} is discharged. During this state, fault restoration should be adequately achieved. After fault restoration, the operation state is returned to State 1.

3. Simulation Results

Table 1. Simulation parameters.

Symbol	Quantity	Value
V_{in}	Input voltage	100[V]
R_{load}	Load resistor	32[Ω]
C_{pri} and C_{sec}	Charging capacitor	10.5[μF]
R_{para_p} *and* R_{para_s}	Parallel resistor	0.4[Ω]
R_{seri_p} *and* R_{seri_s}	Series resistor	from 0.5[Ω] to 3[Ω]
L_{line_in} and L_{line_out}	Line impedance	66[μH]
L	Self-inductance	580[μH]
K	Coupling coefficient	0.96
L_{lk}	Leakage inductance	22[μH]
t_2	The time at a short-circuit fault	at 2[ms]
T_{delay}	Interval time	20[μs]

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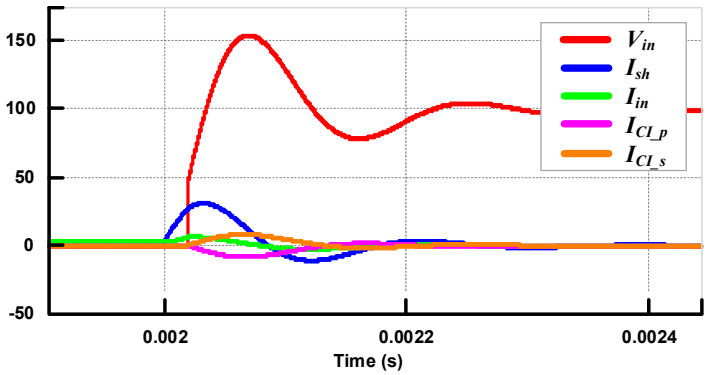

Figure 4. Key waveforms of simulation results

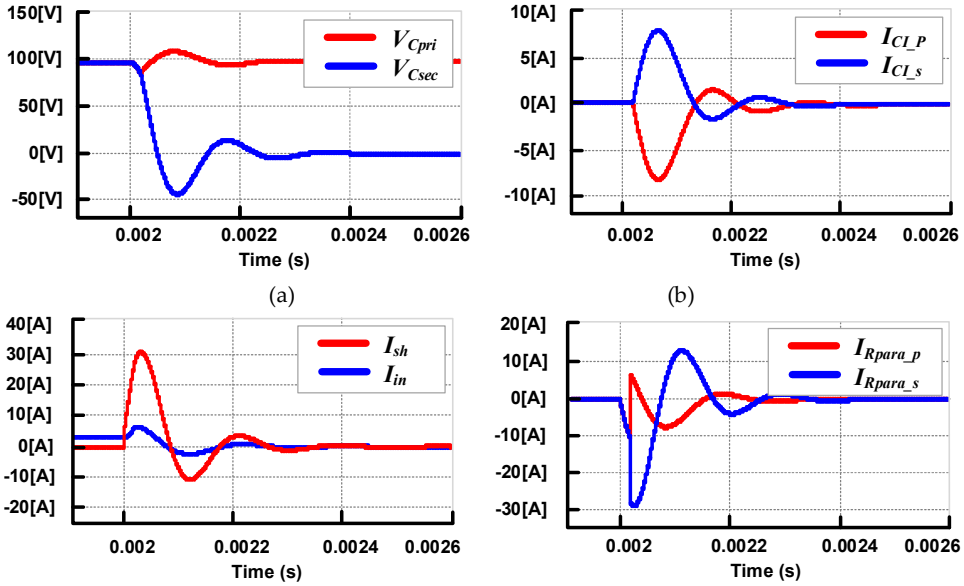

Figure 5. Simulation waveforms of commutation capacitors and the coupled inductor: (a) voltages across commutation capacitors, (b) coupled inductor currents, (c) currents of input and short-circuit fault and (d) parallel resistor currents.

To verify the effectiveness under a pole-to-ground short-circuit fault, the SSCB-CI is simulated in PSIM. Detailed simulation parameters are listed in Table 1. As mentioned in section 2, the parasitic components of the CI and the capacitors are neglected for ease of analysis. Also, only the short-circuit fault on the load side is considered.

Fig. 4 shows representative waveforms under operation states from stationary to protection, Where R_{seri_p} and R_{seri_s} are considered as 1[Ω]. After an interval time of 20[μs], V_{sw} is clamped to an adjustable voltage level of SW_{main}. At the same time, I_{in} is interrupted by the turn-off switch, and I_{sh} reaches the peak level. After starting to oscillate, I_{sh} is reduced gradually to zero.

Fig. 5 shows enlarged simulation waveforms of commutation capacitors and each winding of CI. As shown in Fig. 5 (a), V_{Cpri} does not become zero because of impressed input voltage continuously. However, V_{Csec} becomes zero because of truned-off of SW_{main}. Fig. 5 (b) shows the current waveforms in the coupled inductor, which means the current reflected to each winding under short circuit fault.

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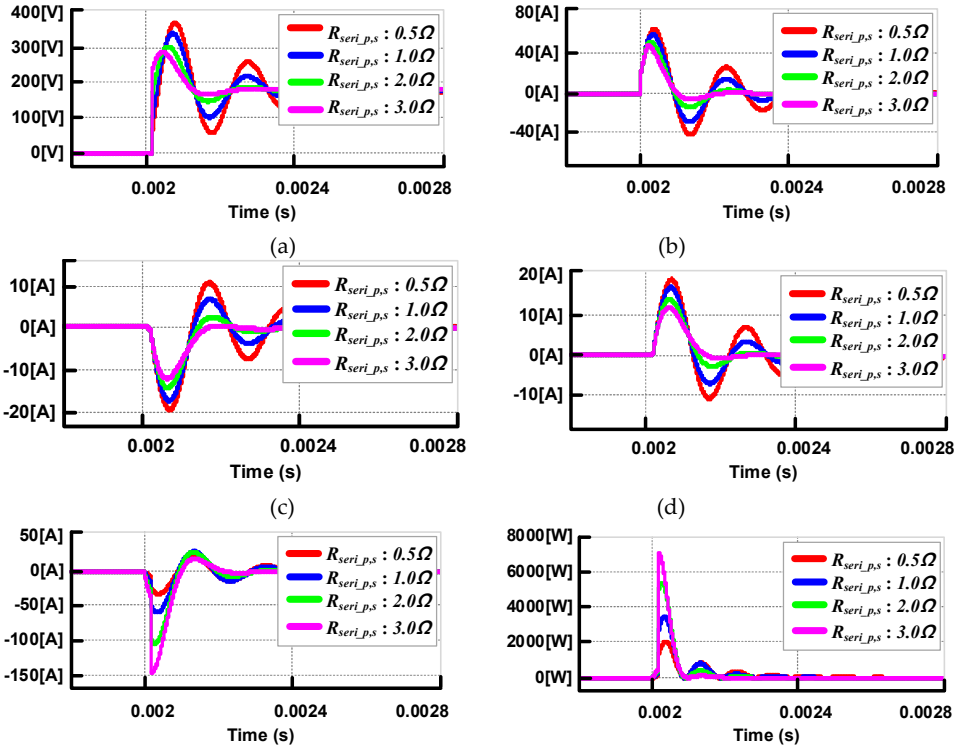

Figure 6. Simulation waveforms for different series resistor values: (a) voltage across main switch, (b) fault current, (c) current in primary winding, (d) current in secondary winding, (e) current of parallel resistor linked to secondary winding, and (f) power burden of series resistor linked to secondary winding

Fig. 6 indicates simulation waveforms under the different R_{seri_p} and R_{seri_s} values from 0.5[Ω] to 3.0[Ω]. Its waveforms show the better characteristic when R_{seri_p} and R_{seri_s} are selected as high resistance ranges. However, this range selection causes more power burden of resistors.

The peak of the voltage and current peak should be clamped within the allowable level of the main switch. In this paper, it is possible to explore an allowable level by selecting the value of R_{seri_p} and R_{seri_s}. Also, the clearing time can be reduced correspondingly according to the resistance values. Fig. 6 shows the output characteristic when R_{seri_p} and R_{seri_s} are set respectively from 0.5[Ω] to 3[Ω]. Under same simulation parameters indicated in Table 1, the results reveal the increase in V_{sw} and I_{sh} as the under-damping by lower resistance value, and the clearing time is increased. On the contrary, V_{sw} and I_{sh} decrease as over-damping by higher resistance value, and the clearing time is decreased. However, the over-damping condition has a disadvantage in that the power burden of R_{seri_s} to consume the fault current is increased, which increases the resistor size and rated power to circuit configuration. Therefore, selection of appropriate resistance value of R_{seri_p} and R_{seri_s} between under damping and critical damping should be explored. In another solution, the power burden of the resistor can be reduced by selecting a high k value.

Fig. 7 shows the waveforms according to k value over the range of 0.36 to 0.96 in accordance with transient oscillation in a magnitude of I_{Cl_p} and power burden of R_{para_s}. As the k value increases, the current magnitude increases, which decreases the power burden of R_{para_s}.

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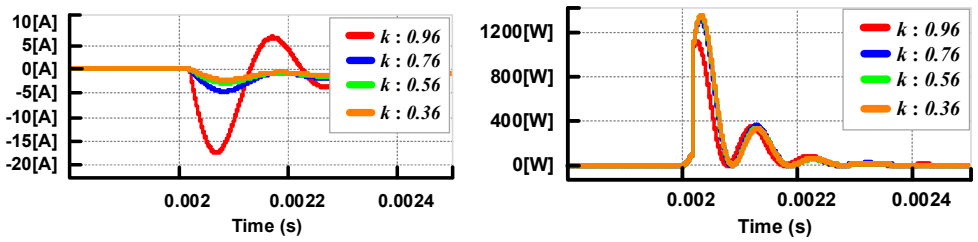

(a) (b)

Figure 7. Simulation waveforms for different coupling coefficients: (a) current in secondary winding, and (b) power burden of parallel resistor linked to secondary winding.

4. Experimental Results

Based on the simulation results, a lab-scale prototype has been built in order to verify the performance of the proposed SSCB-CI. The test conditions and detailed parameters of the CI are considered in Tables 2 and 3, respectively, where the core shape is selected as ferrite PQ core. In this paper, fault detection condition is regarded as being when the MCU detects the input current above the limit current level. The prototype SSCB-CI is composed of FF150R12RT4 IGBT module, three PMC 700[V]/5[uF] capacitors in parallel and DSP TMS320F28335, where ADC frequency is set as 40[kHz].

Table 2. Parameters of experimental condition.

Symbol	Quantity	Value
V_{in}	Input voltage	100[V]
Z_{line_in} and Z_{line_out}	Line impedance	66[μH]/0.2[Ω]
C_{in}	Input capacitor	3200[μF]
SW_{main}	Main switches	1200 [V]/ 150[A]
C_{pri} and C_{sec}	Commutation capacitor	15[μF]
R_{para_p} and R_{para_s}	Parallel resistors	0.4[Ω]
R_{seri_p} and R_{seri_s}	Series resistors	1[Ω]
T_{delay}	Time delay	about 190[μs]
f_{ADC}	ADC frequency	40[kHz]

Table 3. Parameters of coupled inductor

Symbol	Quantity	Value
k	Cou sharplypling coefficient	0.96
L	Self inductance	680[μH]
L_m	Magnetizing inductance	652.8[μH]
L_{lk}	Leakage inductance	27.2[μH]

Table 4. Specifications of measurement sensors and instruments

Item	Model
DC power supply	N8957APV
Voltage sensor	LV25P
Current sensor	LA100-P
DSP	TMS320F28335
Main switch	FF150R12RT4
Oscilloscope	Waverunner 44MXi

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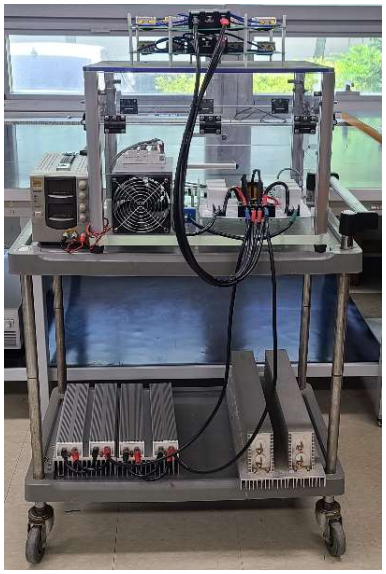

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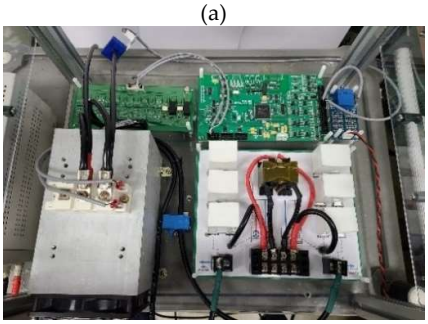

(b)

Figure 8. Experimental set-up of the SSCB-CI: (a) overall test circuit configuration, and (b) inner structure

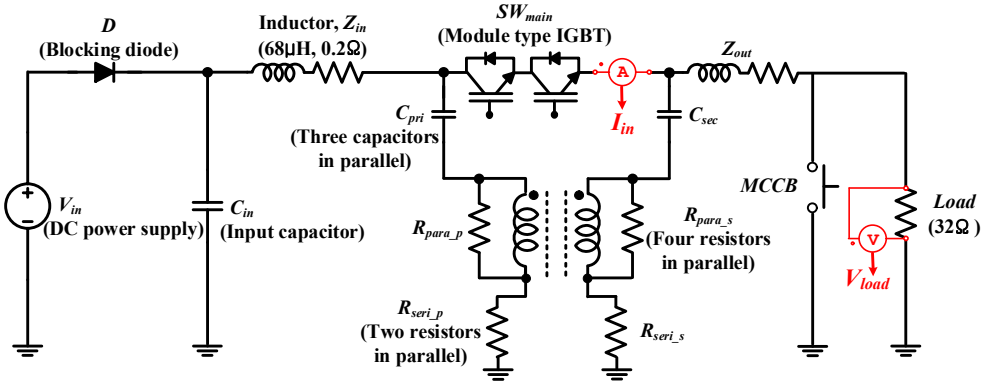

Figure 9. Test circuit schematic for the short-circuit scheme.

The overall testing configuration is built as shown in Fig. 10 (a). Fig. 10 (b) shows the prototype SSCB-CI configuration, which consists of an IGBT module, a gate driver, an MCU board, capacitors and a CI.

The detailed short circuit test setup and overall configuration of main components are designed as shown in Fig. 9. Where, sensing parts of current and voltage value is indicated in red.

The sequence for short circuit scheme is as follows: Input capacitor C_{in} is charged in advance by AC/DC power supply under constant voltage constant current (CVCC) mode at 100[V] via input side blocking diode, D which has the role to block inverse current to the power supply. After that, the SSCB-CI is operated in State 1. In order to force pole-to-

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ground short-circuit fault, MCCB is turned on. Under this condition, there is a time delay of about 190[μs]. The microcontroller unit measures the main switch voltage and the current to decide pole-to-ground fault condition. If the fluctuation range of V_{sw} and I_{in} is over a certain value, it is judged as a short circuit fault.

Fig. 10 shows the overall test results of the SSCB-CI from initial condition to state 6, where R_{seri_p} and R_{seri_s} are set as 1[Ω]. Fig. 10 (a) indicates major experiment results and enlarged waveforms at a condition of intended fault accident. Also, Fig. 10 (b) shows voltage waveforms and current waveform at State 1. Once the power supply is turned on, V_{Cpri} is charged, and V_{in} is blocked because of SW_{main} turned off. Therefore, V_{Csec} is sustained by zero. At this time, each current of R_{para_p} and R_{para_s} flows momentarily, as shown in Fig. 12 (c). After SW_{main} turns on, V_{Csec} is charged as V_{in}. At this state, I_{in} start to flows to the load. Fig. 12 (e) and (f) show the resulting waveforms from State 3 to State 6. In these figures, waveforms show across voltages and commutating currents into main components of SSCB-CI circuit after short-circuit fault. At initial time of state 5, V_{sw} increases rapidly up to 1.5 times of V_{in}. However, V_{sw} reduces up to input voltage value after clearing time like State 5.

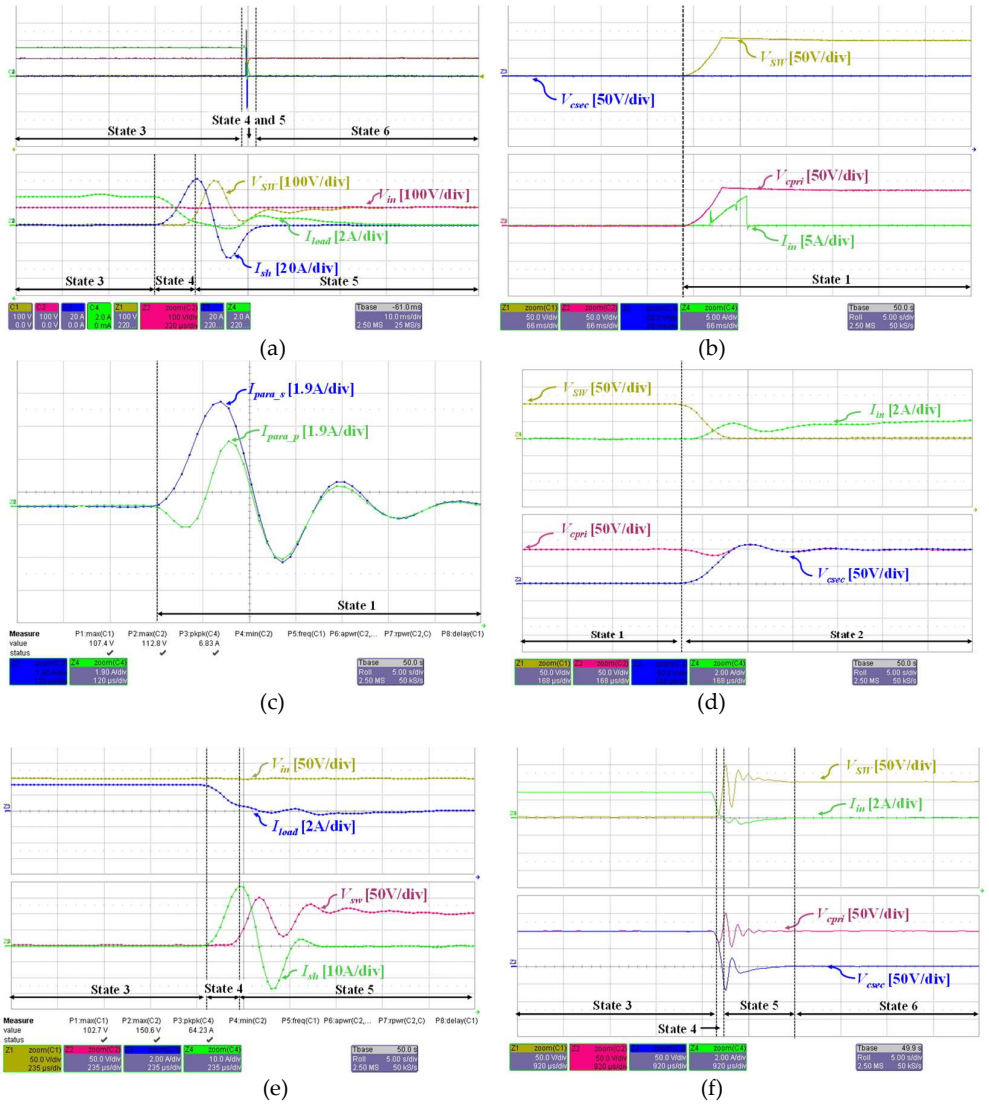

Figure 10. Experimental waveforms under overall operation states: (a) Key waveforms of experimental results (b) switch, capacitor voltages and input current under state 1, (c) parallel resistor current under state 1, (d) switch, capacitor voltage and input current under state 2, (e) input, switch

voltage and load, fault current under state 4, and (f) switch, capacitor voltage and input current under states 4 and 5.

5. Conclusion

This paper explores the circuit configuration of solid-state DC circuit breaker with CI and the applicability in short-circuit fault. In the circuit configuration, several passive components are considered for reducing the number of power semiconductor devices as a substitute for a complex circuit configuration in the early versions of the proposed SSCB. The operation states are analyzed to determine the overall voltage and current flow in the proposed circuit. The results indicate that the considered resistor value leads to a blocking voltage level of main switches and clearing time of the fault current. The effectiveness of the SSCB-CI is verified through simulation and experimental results. In simulation results, it is founded that the coupling coefficient affects the power burden of parallel-linked resistors. In the experimental configuration, circuit configuration of SSCB-CI as the small-scale prototype is implemented. Presented results demonstrate the functionality of blocking the fault current under pole-to ground fault in DC distribution. The rating power and blocking voltage of the devices used in the circuit are designed to be comparatively high. This intention caused problems about bulky size and increased weight by series or parallel configuration of components. Considering the implemented prototype scale, future research needs to verify the effectiveness of the full-scale SSCB-CI for a practical DC microgrid and size optimization.

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