Multi-channel Precision Voltage Source for Experiments on Quantum dots

Yumei TANG [1, 2*], Kefu LIU [1]

(1. School of Information Science and Technology, Fudan University, No.220 Handan Road, Shanghai, 200433, P.R. China

2.Hefei GoodTech Co., Ltd., Anhui, Hefei, 230088)

*Corresponding author: goodtek0551@163.com

Abstract:

To realize precise control of single quantum dots (Qdots) device, the high-performance bias source play the key role. In this paper, the 16-channel high precision voltage bias source prototype for Qdots device with 18-bit resolution was designed. The prototype was made and its performance was tested. The short time fluctuations can reach 50μV. The up-step and the down-step response time can achieve less than 3μs. The stability, linearity and setting time of the bias source exhibits good performance. What's more, the voltage bias source can be controlled by local and online. The results show that it is one effective and feasible topology for the high precision voltage bias source in Qdots device application.

Keywords: quantum dots; *bias source; Multi-channel, high precision*

Introduction:

Recently, as many fundamental properties are size dependent in the nanometer range, a great deal of attention has been focused on the optoelectronic properties of quantum dots (Qdots)[1-4]. Qdots is one of most significant basic structures of nano-electronics which is regarded as development direction of the next generation semiconductor devices to replace traditional semiconductor technology[5, 6]. The Qdots device was widely investigated for quantum computing[7, 8], quantum detection[9, 10], quantum communication[11, 12] and quantum measurement[13-16].

In general, it is necessary to apply bias voltage on the gate of quantum dots to empty the two-dimensional electron gas below them and form quantum dots or quantum dot contact channels[17]. The Qdots device is mostly general driven by electric including current and voltage bias[18, 19]. The stability, linearity and setting time of bias source are key factors to affect the Qdots device performance[20-23]. In order to realize precise control of single quantum dots and quantum channels, it is meaningful to investigate on the high precision and quality bias source for Qdots device.

To our knowledge, the existing instruments are large volume with few channels or with limited accuracy[24, 25], meanwhile multi-channel and high precision bias voltage source is rarely reported in the literature. ADI recommends to use high resolution DAC chip to design the bias voltage source[26, 27]. Although precision DAC components are already on the market, building a multi-channel high-resolution system is not easy and cannot be treated hastily. The sources of error must be fully considered, which occur

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 20 July 2021 doi:10.20944/preprints202107.0458.v1

at this level of accuracy. In high-resolution circuits, the main error sources are noise, temperature drift, thermoelectric voltage, and physical stress. The construction technology of precision circuits should be followed to minimize the coupling and propagation effects of such errors in the entire circuit and avoid external interference. To further complicate the issue, mixed-signal ICs have both analog and digital ports, and because of this, much confusion has resulted with respect to proper grounding techniques. In addition, some mixed-signal ICs have relatively low digital currents, while others have high digital currents. In many cases, these two types must be treated differently with respect to optimum grounding[28].

design and analysis:

1)system design

As shown in Fig.1, this system was consisted of digital circuit, analog circuit, LCD & keys, AC-DC power and PC communication system. With the main controller (MCU, STM32F405) as the core, the precision digital-to-analog converter (AD5781 ,18-bit DAC) is used to complete the design of the precision voltage source. The voltage value is transmitted to the MCU by the user through ethernet or keys input to read and write voltage commands to the corresponding channel for decoding and matching, and the decoded data and synchronization signal are simultaneously input to the precision digital-to-analog conversion circuit, and finally measure the final voltage with a high-precision multi-meter (Agilent 3458A), and use the correction model to achieve the calibration of the offset voltage.

The key point of the circuit design is to completely separate the digital circuit and the analog circuit, and use independent power and ground processing, and the signal transmission between the two is isolated from each other through the optocoupler, so as to ensure that the digital circuit noise does not enter the analog circuit.

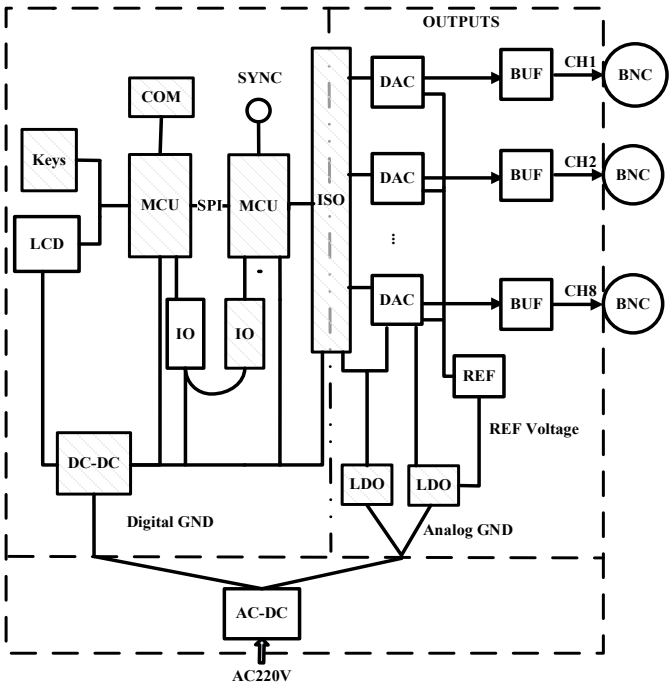

Fig.1. system block

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 20 July 2021 doi:10.20944/preprints202107.0458.v1

The output voltage expression[29] of 18bit DAC is:

$$V_{out} = \frac{(V_{refp} - V_{refn}) * D}{2^{18} - 1} + V_{refn} \quad (1)$$

where:

Vrefn provides a negative reference voltage for the DAC;

Vrefp provides a positive reference voltage for the DAC;

D is an 18-bit binary programming value.

2) Output voltage accuracy and temperature drift analysis

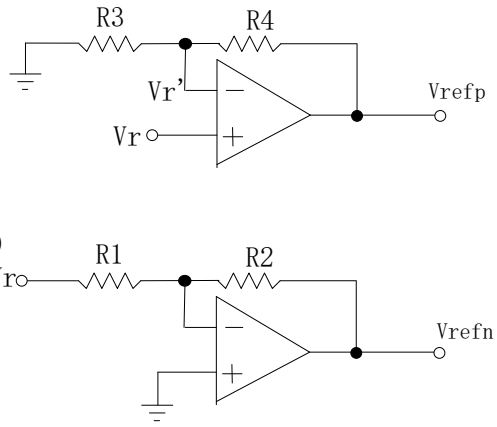

Fig.2. (a) Positive polarity reference voltage generating circuit ;(b) Negative polarity reference voltage generating circuit

As shown in Fig 2(a), Vr is the reference voltage, we choose the ultralow noise, LDO XFET voltage references with current sink and source(adr445B, ADI), temperature coefficient is 2ppm,the output voltage is 5V±2mV.

Regardless of the influence of the op amp bias current, assuming that the op amp offset voltage is Vos1, let Vr'=Vr+Vos1, according to the "virtual disconnection" principle, the following formula：

$$\frac{V_r'}{R3} = \frac{V_{refp} - V_r'}{R4} \quad (2)$$

So that,

$$V_{refp} = \left(1 + \frac{R4}{R3}\right) V_r' \quad (3)$$

As shown in Fig 3(b), assuming that the op amp offset voltage is Vos2, let Vr''=Vr+Vos2, and the same can be obtained:

$$\frac{V_r''}{R1} = \frac{-V_{refn}}{R2} \quad (4)$$

$$V_{refn} = -V_r'' * \frac{R2}{R1} \quad (5)$$

Where :

Vrefn provides a negative reference voltage for the DAC;

Vrefp provides a positive reference voltage for the DAC.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 20 July 2021 doi:10.20944/preprints202107.0458.v1

Substituting formula (2), (3), (4), (5) into formula (1), we can get:

$$V_{out} = \left(\left(1 + \frac{R4}{R3}\right) * (Vr + Vos1) + \frac{R2}{R1} * (Vr + Vos2)\right) * \frac{1}{2^{18}-1} * D - \frac{R2}{R1} * (V_r + Vos2) \quad (6)$$

Assuming that R2/R1, R4/R3, Vr, Vos1, Vos2 do not change with temperature and time, Vout can be simplified to:

$$Vout = a * D + b \quad (7)$$

Here, R1, R2, R3, R4 use Vishay bulk metal thin film voltage divider resistor series 300144Z and 300145, its resistance tracking temperature coefficient is 0.1 ppm/°C.

It can be seen from the above formula that the bias output voltage will be affected by the drift of the DAC, resistance, reference voltage, and operational amplifier.

The reference voltage source adopts ADR445BRZ to output 5V, and the temperature drift is about 2ppm/℃, which is 10 uV/℃.

The temperature drift of the voltage divider resistance is about 2ppm, and the temperature drift of the voltage divider resistance is required to be consistent, and the tracking temperature coefficient is less than 5 uV/℃.

The offset drift of AD8676 is about 0.6 μV/°C. AD5781 has a very low temperature coefficient of about 0.05ppm/°C, which is much lower than the drift of the reference voltage source.

Ignoring the temperature drift of the op amp and DAC, it is mainly affected by the reference voltage source, and the drift is about 20 uV/°C.

Generally speaking, for a 20V voltage range, 18-bit system, the temperature drift is required to be controlled within 80uV, and the temperature cannot change more than 4 degrees.

3) Capacitive load analysis

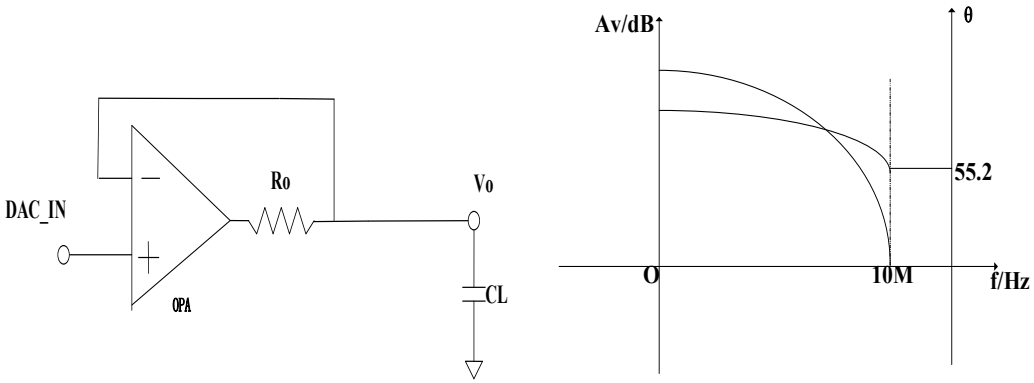

Fig.3. (a) DAC BUF design (b) AD8676 Bode Plots

The ideal operation state of the operational amplifier is that the output voltage and the input voltage are in phase, that is, when the Inca voltage at the negative input causes the output to increase, the operational amplifier can correspondingly reduce the increased voltage. However, the input and output phases of operational amplifiers are always different. When the phase difference between the output and the output is

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 20 July 2021 doi:10.20944/preprints202107.0458.v1

180 ° The negative input is exactly the same as the positive input, but the output that should be reduced is enhanced（ It becomes a state of positive and negative collapse.) If it falls into this state in a certain frequency band and remains the original amplitude, the output frequency and oscillation state will continue.

$$A_{Cl}=\frac{Uo}{Ui}=\frac{Zo}{Ro}=-j*\frac{1}{2*pi*CL*f*Ro} \quad (6)$$

While Acl= 1 ， $fp=\frac{1}{2*pi*CL*Ro}>10$ MHz ；

While fp > 10 MHz, Ro >40 Ω , CL <400 pF， there will be no shock.

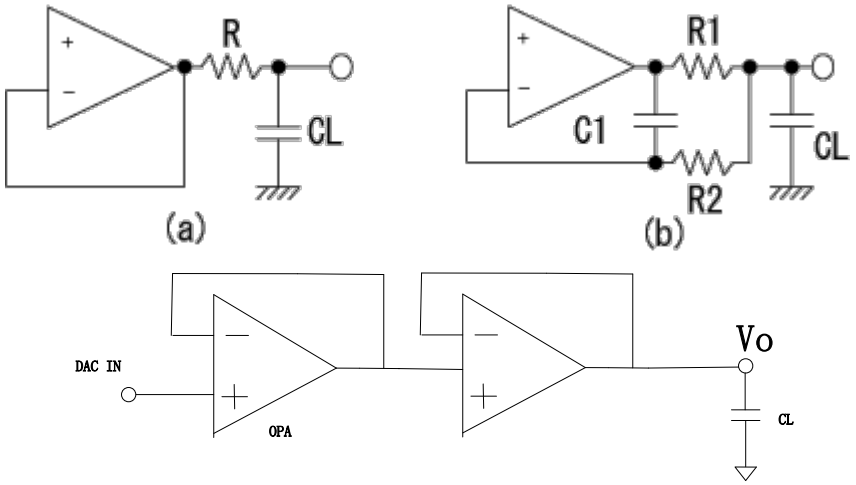

Fig.4 (a) Insert resistance R (b). Miller effect compensation (c) Stretch bandwidth

Fig.4(a) R is inserted in the figure to eliminate the phase lag of feedback loop due to CL

In high frequency region, R is shown as the load of operational amplifier replaces CL. Although R is added to the outside of the feedback loop, the series resistance R can act on the transfer function of the feedback network by the additional zero frequency FZ generated by the load capacitance, thus reducing the phase shift of the high frequency loop. In order to ensure the stability of the circuit, the value of R should make the additional zero frequency at least 10 times lower than the closed-loop bandwidth of the op amp circuit.

Fig.4(b) Miller effect compensation

The phase lag caused by CL is eliminated by pre-correction and C1 insertion.

Fig.4(c) Two stage OPA extended bandwidth

The phase delay caused by CL is compensated by the advanced correction, which is equivalent to adding a buffer at DAC output stage, and responding in time to the first stage operational amplifier response.

Results and discussion:

The multi-channel precision voltage source (MPVS-X) prototype was shown in Fig.5.The LCD screen and controller were distributed in the front panel layout. The Input-Power, power controller, muti-output, RS232 output interface and network interface were distributed in the rear panel layout. The size of prototype is 437mm*420mm*133mm (3U chassis size).

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 20 July 2021 doi:10.20944/preprints202107.0458.v1

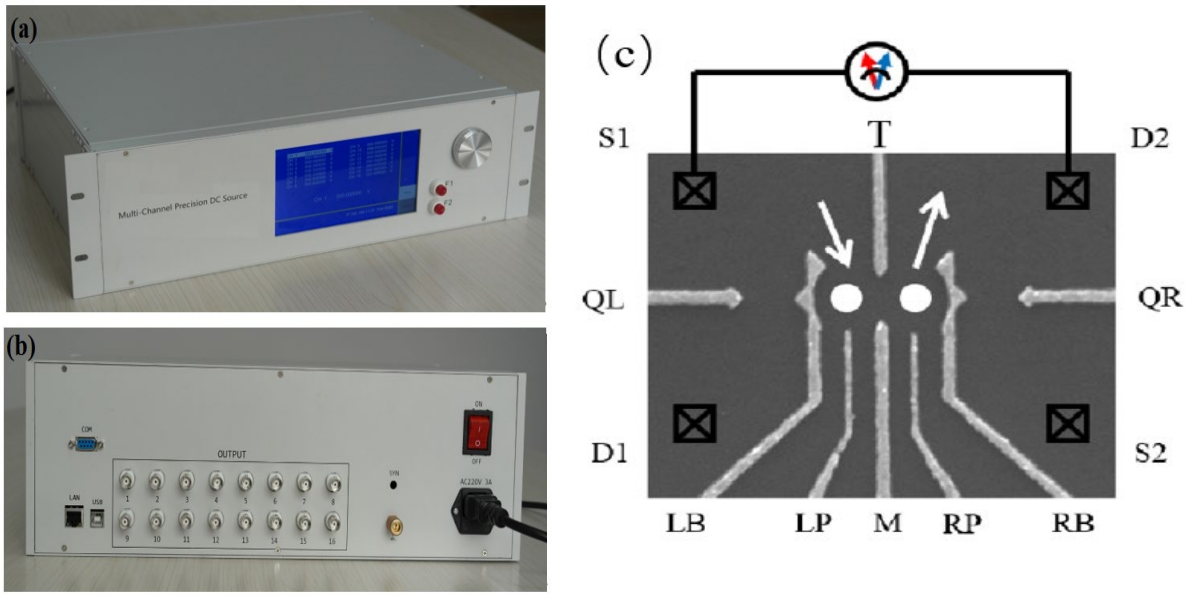

Fig. 5. (a), the front panel layout of prototype; (b) the rear panel layout of prototype; (c) bias source test in Qdots device application

1) Linearity

Set the output of the voltage source in the program, from the minimum value that can be set to the maximum value that can be set, in steps of 10 mV. Wait for 0.5s after setting the voltage value each time, and then use the 8.5-digit digital multi-meter (Agilent 3458A) to read the actual output voltage value. The whole process is repeated 5 times. Save the data of the original set voltage value—the actual voltage value, and perform curve fitting as shown in Fig 6.

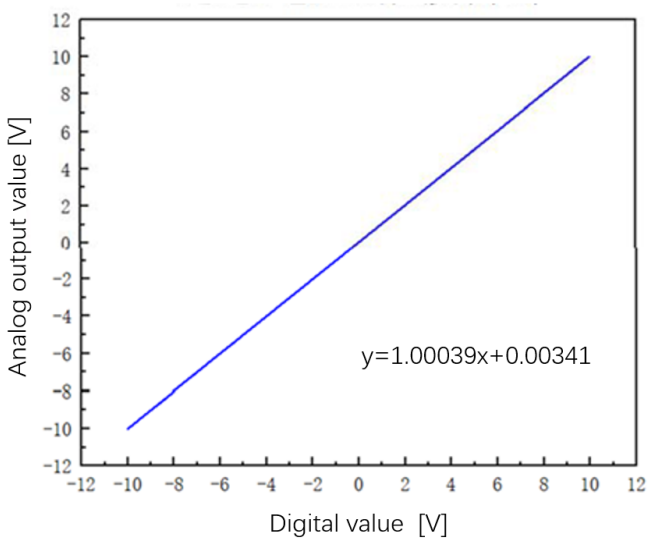

Fig 6 Linear fitting of output voltage

2）Short time fluctuations

Set different voltage output in the program, wait for 0.5s after setting the voltage value each time, and then read the actual output voltage value with an 8.5-digit digital multi-meter (Agilent 3458A), continuously measure 100 s, and count the peak-to-peak voltage jitter. The whole process is repeated 5 times.

Table 1. *Output voltage fluctuations under different voltage*

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 20 July 2021 doi:10.20944/preprints202107.0458.v1

Vout/V	-10	-7.5	-5	-2.5	0	2.5	5	7.5	10
Fluctuations /μV	45.8	36.8	26.6	13.3	1.4	11.3	32.7	28.1	39.2

The voltage output range of this system is -10V~10V. For 18-bit system, 1 LSB is 76μV, and the maximum voltage jitter does not exceed 50μV in the full voltage range.

3) Uniformity between two channels

As shown in Fig.7, the two channels have the same set voltage of - 5.5V and - 1V respectively, and read the actual output voltage value with an 8.5-digit digital multi-meter (Agilent 3458A)，continuously measure for a long time.

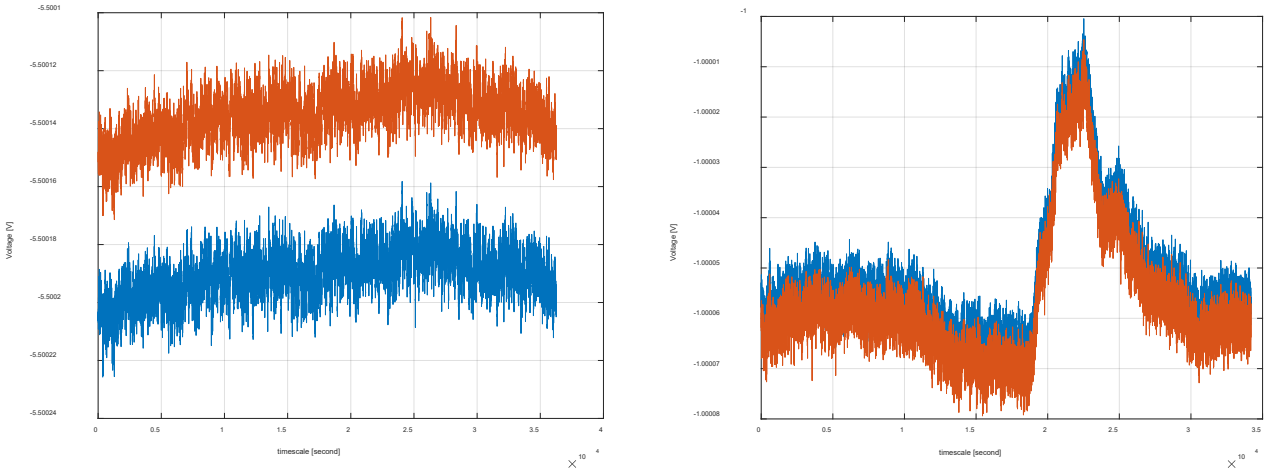

Fig.7 the uniformity between different channels

4) Step response

As shown in Fig.8，The step is set from -5V to +5V. According to the test results of the oscilloscope, the 10V step has a settling time of about 2.4~2.7us.

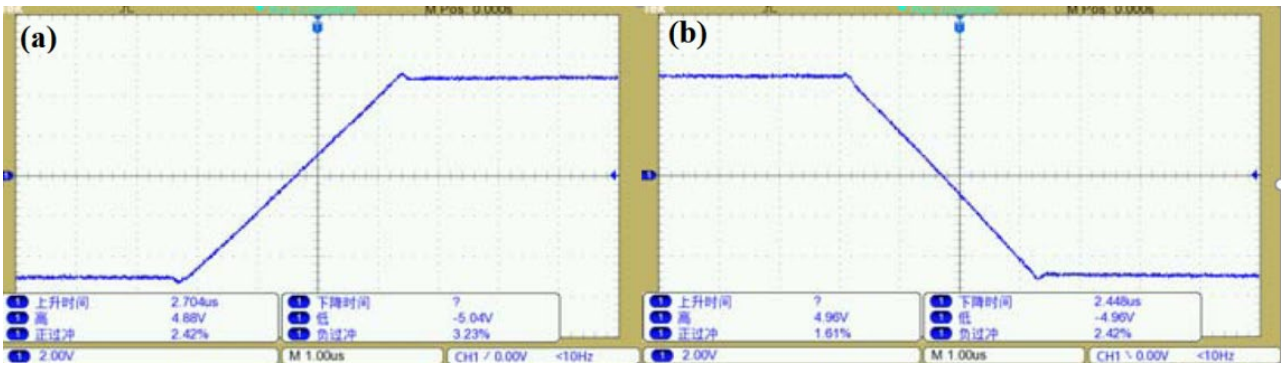

Fig 8 (a)-5V~+5V step response (b)+5V~-5V step response

5）Long-term stability

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 20 July 2021 doi:10.20944/preprints202107.0458.v1

Turn on the output of 16 test channels at the same time and set their voltage output to 10 V at the same time, test the voltage value of random channels among them, read it every 10s, and the test duration is 24 hours. The output voltage change curve with time is as follows:

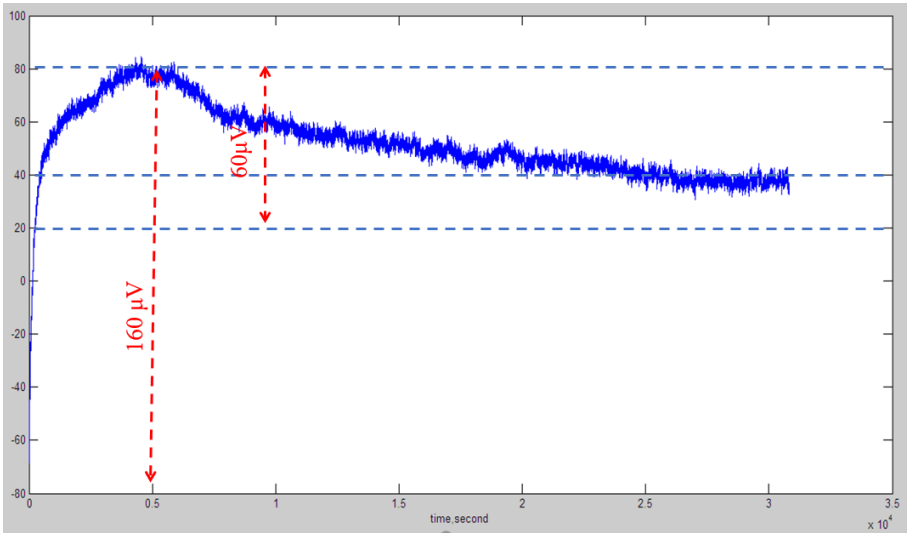

Fig. 9 the output voltage stability test

The output stability of the system was show in the Fig.9. After starting up and running for about 2 hours, the internal temperature of the instrument gradually rises, and the output voltage will drift by 160μV, and then the internal environment of the instrument gradually stabilizes. When multiple channels work at the same time, the system has excellent long-term stability of voltage output and maximum fluctuation. The range is less than 20 μV.

Conclusion:

Multi-channel bias voltage source technology is a typical technology of low noise circuit design, involving resolution, noise, accuracy, linearity, temperature, channel consistency, bias, long-term stability, low complexity and other aspects. The project research focuses on these problems closely, and achieves 4ppm conversion accuracy by designing high-resolution digital to analog conversion circuit; Through scientific exploration, a series of low noise circuit design problems such as power supply, grounding processing and signal isolation are solved; Through closed-loop measurement and digital correction, accurate voltage output is obtained; The problem of capacitive load and linearity is solved by two-stage op amp output; Through careful heat dissipation, the whole machine controls the temperature change on the one hand; On the other hand, the temperature drift of components is very low, which minimizes the temperature drift coefficient of the system and improves the working temperature range through temperature compensation; Through careful structure design of the whole machine, the complexity of the system is reduced, and the humanized man-machine interface is realized. The results show that it is one effective and feasible topology for the high precision voltage bias source in Qdots device application.

References

1. Wu, J., Chen, S., Seeds, A., and Liu, H., 'Quantum Dot Optoelectronic Devices: Lasers, Photodetectors and Solar Cells', *Journal of Physics D: Applied Physics*, 2015, 48, (36), p. 363001.
2. Bekhouche, H., Rahou, D., Gueddim, A., Abdelhafidi, M.K., and Bouarissa, N., 'Electron States, Effective Masses and Transverse Effective Charge of Inas Quantum Dots', *Optical and Quantum Electronics*, 2018, 50, (8), p. 309.
3. Kim, Y., Kim, J.O., Lee, S.J., and Noh, S.K., 'Submonolayer Quantum Dots for Optoelectronic Devices', *Journal of the Korean Physical Society*, 2018, 73, (6), pp. 833-840.
4. Min, X., Pengchen, Z., Gu, S., and Jia, Z., 'Research Progress of Low-Dimensional Perovskites: Synthesis, Properties and Optoelectronic Applications*', *Journal of Semiconductors*, 2016.
5. Chung, Y., Choi, J., and Sim, H.S., 'Electron Transport in a Multiple Quantum Dot: Recent Progress', *Journal of the Korean Physical Society*, 2018, 72, (12), pp. 1454-1466.
6. Iravani, S. and Varma, R.S., 'Green Synthesis, Biomedical and Biotechnological Applications of Carbon and Graphene Quantum Dots. A Review', *Environmental Chemistry Letters*, 2020, 18, (3), pp. 703-727.
7. Wilson and Mark, R., 'Silicon-Based Quantum Dots Have a Path to Scalable Quantum Computing', *Physics Today*, 2018, 71, (4), pp. 17-20.
8. Bonen, S., Alakusu, U., Duan, Y., Gong, M.J., Dadash, M.S., Lucci, L., Daughton, D.R., Adam, G.C., Iordănescu, S., Pă şteanu, M., Giangu, I., Jia, H., Gutierrez, L.E., Chen, W.T., Messaoudi, N., Harame, D., Müller, A., Mansour, R.R., Asbeck, P., and Voinigescu, S.P., 'Cryogenic Characterization of 22-Nm Fdsoi Cmos Technology for Quantum Computing Ics', *IEEE Electron Device Letters*, 2019, 40, (1), pp. 127-130.
9. Kurzmann, A., Overweg, H., Eich, M., Pally, A., Rickhaus, P., Pisoni, R., Lee, Y., Watanabe, K., Taniguchi, T., Ihn, T., and Ensslin, K., 'Charge Detection in Gate-Defined Bilayer Graphene Quantum Dots', *Nano Letters*, 2019, 19, (8), pp. 5216-5221.
10. Ihn, T., Gustavsson, S., Gasser, U., Küng, B., Müller, T., Schleser, R., Sigrist, M., Shorubalko, I., Leturcq, R., and Ensslin, K., 'Quantum Dots Investigated with Charge Detection Techniques', *Solid State Communications*, 2009, 149, (35), pp. 1419-1426.
11. Simon, C., Niquet, Y.-M., Caillet, X., Eymery, J., Poizat, J.-P., and Gérard, J.-M., 'Quantum Communication with Quantum Dot Spins', *Physical Review B*, 2007, 75, (8), p. 081302.
12. Burkard, G., Engel, H.A., and Loss, D., 'Spintronics and Quantum Dots for Quantum Computing and Quantum Communication', *Fortschritte der Physik*, 2000, 48.
13. Cui, W. and Dong, D., 'Modeling and Control of Quantum Measurement-Induced Backaction in Double Quantum Dots', *IEEE Transactions on Control Systems Technology*, 2019, 27, (6), pp. 2499-2509.
14. Yi, X.-F., Xu, P., Yao, Q., and Quan, X., 'Quantum Repeater without Bell Measurements in Double-Quantum-Dot Systems', *Quantum Information Processing*, 2019, 18, (3), p. 82.
15. Liu, J., Jiang, Z.-T., and Shao, B., 'Local Measurement of the Entanglement between Two Quantum-Dot Qubits', *Physical Review B*, 2009, 79, (11), p. 115323.
16. Xue, Z.-Y., 'Measurement Based Controlled Not Gate for Topological Qubits in a Majorana Fermion and Quantum-Dot Hybrid System', *The European Physical Journal D*, 2013, 67, (4).
17. Heinzel, T., Wharam, D.A., Aguiar, F.M.D., Kotthaus, J.P., Bohm, G., Klein, W., Trankle, G., and Weimann, G., 'Current-Voltage Characteristics of Quantum Point Contacts in the High-Bias Regime', *Semiconductor Science & Technology*, 1994, 9, (6), pp. 1220-1225.
18. Coleman, P., Hooley, C., Avishai, Y., Goldin, Y., and Ho, A., 'Oscillatory Instabilities in D.C. Biased Quantum Dots', *Journal of Physics Condensed Matter*, 2001, 14, (8), p. 33013.
19. Mukaiyama, T., Takeuchi, N., Yamanashi, Y., and Yoshikawa, N., 'Design and Demonstration of an on-Chip Ac Power Source for Adiabatic Quantum-Flux-Parametron Logic', *Superconductor Science and Technology*, 2013, 26, (3), p. 035018.
20. Mukaiyama, T., Takeuchi, N., Ehara, K., Inoue, K., Yamanashi, Y., and Yoshikawa, N., 'Operation of an Adiabatic Quantum-Flux-Parametron Gate Using an on-Chip Ac Power Source', *IEEE Transactions on Applied Superconductivity*, 2013, 23, (4), pp. 1301605-1301605.
21. Wulf, M., Ohki, T.A., and Feldman, M.J., 'A Simple Circuit to Supply Constant Flux Biases for Superconducting Quantum Computing', *Journal of Physics: Conference Series*, 2006, 43, pp. 1397-1400.
22. Muller, C.R., Worschech, L., Schliemann, A., and Forchel, A., 'Bias Voltage Controlled Memory Effect in in-Plane Quantum-Wire Transistors with Embedded Quantum Dots', *IEEE Electron Device Letters*, 2006, 27, (12), pp. 955-958.
23. Taranko, R. and Parafiniuk, P., 'Influence of the Coulomb Interaction on the Spin-Polarized Current in the Quantum Dot System in the Presence of the Bias Voltagepulse', *Physica E: Low-dimensional Systems and Nanostructures*, 2013, 49, pp. 5-12.
24. Böhm, C., Sturm, S., Rischka, A., Dörr, A., Eliseev, S., Goncharov, M., Höcker, M., Ketter, J., Köhler, F., Marschall, D., Martin, J., Obieglo, D., Repp, J., Roux, C., Schüssler, R.X., Steigleder, M., Streubel, S., Wagner, T., Westermann, J., Wieder, V., Zirpel, R., Melcher, J., and Blaum, K., 'An Ultra-Stable Voltage Source for Precision Penning-Trap Experiments', *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 2016, 828, pp. 125-131.
25. Saulnier, G.J., Ross, A.S., and Liu, N., 'A High-Precision Voltage Source for Eit', *Physiol Meas*, 2006, 27, (5), pp. S221-236.
26. Lynch, M., 'High Precision Voltage Source', *Analog Devices, Inc*, 2017.
27. Egan, M., 'The 20-Bit Dac Is the Easiest Part of a 1-Ppm-Accurate Precision Voltage Source', *Analog Dialogue*, 2010, 44, (4), p. 1.

 doi:10.20944/preprints202107.0458.v1

28. Kester, W., Bryant, J., and Byrne, M., 'Grounding Data Converters and Solving the Mystery of" Agnd" and" Dgnd', *Analog Devices Tutorial*, 2009.
29. True, A. and Bit, V.O.D., '18-Bit, Linear, Low Noise, Precision Bipolar±10 V Dc Voltage Source'.