Black-Box Modeling Approach with PGB Metric for High-Frequency PSRR Prediction in Op-Amps

Yi Zhang * , Xin Yang , Ruonan Lin , Tailai Li

Posted Date: 17 March 2025

doi: 10.20944/preprints202503.1187.v1

Keywords: PGB; op-amps; PSRR; Thevenin Equivalence

Article

Black-Box Modeling Approach with PGB Metric for High-Frequency PSRR Prediction in Op-Amps

Yi Zhang [1,*], Xin Yang [2], Ruonan Lin [3] and Tailai Li [4]

[1] School of Advanced Manufacturing, Fuzhou University, Quanzhou 362251, China; 852203429@fzu.edu.cn
[2] School of Advanced Manufacturing, Fuzhou University, Quanzhou 362251, China; 852303415@fzu.edu.cn
[3] School of Advanced Manufacturing, Fuzhou University, Quanzhou 362251, China; 852201412@fzu.edu.cn
[4] Hangzhou Zhicun (Witmem) Technology Co., Ltd, Shanghai, 201210, China; litailai2021@163.com
* Correspondence: 852203429@fzu.edu.cn; Tel.+86 18205915429

Abstract: The rapid development of electronic technology has generated the demand for low - power and high- performance circuit design. The key indicator, power supply rejection ratio (PSRR), is crucial for circuit design. Given the deficiencies of existing PSRR calculation methods in high-frequency applications and complex circuit designs, this paper proposes an innovative PSRR calculation theory. Based on a simplified circuit model, this theory uses Thevenin's equivalent principle to transform multi-stage operational amplifiers into a black-box model, simplifying the calculation process and enhancing the intuitiveness of calculation. In view of the characteristics of industrial design, we also proposed the PSR Gain Bandwidth (PGB) theory, which can more intuitively analyze the trade-off between PSRR and other performance within the target range. This paper further explores the impact of different circuit structures on PSRR characteristics, covering typical circuit structures such as PMOS/NMOS input two-stage operational amplifiers and folded cascode operational amplifiers, and deeply analyzes the key factors affecting PSRR characteristics. The effectiveness of the proposed theory is verified through case analysis, and its potential applications in circuit designs with high PSRR requirements are demonstrated.

Keywords: PGB; op-amps; PSRR; Thevenin Equivalence

1. Introduction

The swift advancement of electronic technology has given rise to the necessity for low-power and high-performance circuit design [1–4]. In this context, fundamental building blocks of any chip, such as operational amplifiers, low-dropout regulators (LDOs), and bandgap references, have become increasingly important. Maintaining circuit stability under diverse operating conditions thus becomes critical. The PSRR serves as a key metric for assessing a circuit's ability to suppress power supply noise, directly impacting signal integrity and system stability. In the realm of high-precision medical devices [5], enhancing the PSRR augments measurement precision and diagnostic reliability. In high-speed communication systems, it attenuates noise interference during data transmission. And in portable devices, it prolongs battery life and enhances immunity to interference.

Conventional PSRR calculation methods rely predominantly on simplified analyses of system poles and zeros, often using low-frequency equivalent circuit models. However, as circuits operate at higher frequencies, parasitic capacitance, inductance, and other high-frequency effects introduce significant deviations between calculated and actual performance. This discrepancy becomes even more pronounced in radio frequency (RF) and high-speed communication circuits, where complex interactions between power supply noise and parasitic parameters exacerbate the issue. Moreover, existing methods lack a unified theoretical framework and standardized calculation process, forcing designers to invest substantial time in theoretical derivation and experimental validation when addressing novel circuit architectures. Such constraints hinder design efficiency and innovation.

 doi:10.20944/preprints202503.1187.v1

To overcome these challenges, we propose a novel PSRR calculation theory. Our approach evaluates the PSRR of a two-stage operational amplifier by modeling the first stage as a black box with defined input and output. We apply the Thevenin equivalent model to capture the internal behavior of the first stage and reintegrate this result into the overall circuit model. This strategy simplifies the calculation and enhances its intuitiveness. In addition, the proposed theory offers a detailed description of key parameters—including poles, zeros, and gain bandwidth.

Furthermore, industrial design pays more attention to the analysis of power supply rejection ratio (PSR). Since it involves complex S-parameter models, it is difficult to optimize it directly. This paper proposes a simplified evaluation method based on PGB, which avoids the tedious S-parameter calculation by directly extracting PSRR and first-order pole characteristics, thereby achieving efficient and intuitive PSR performance prediction within the target frequency band. This method shows universality before the gain-bandwidth product (GBW), and can uniformly explain the phenomenon that different circuit architectures (such as LDO) have differentiated UGB-level PSR characteristics under the same low-frequency PSR and pole configuration.

We validate the proposed method by analyzing typical circuit structures. The rest of this paper is organized as follows. Section II reviews the traditional PSRR calculation methods and introduces the theoretical basis of our method and details the PSRR calculation process and zero-pole characteristics of different circuits. Section III verifies the accuracy of PSRR calculation through the design and simulation of complex circuits and confirms the feasibility of optimizing PSRR through PGB calculation analysis. Finally, Section IV summarizes the advantages of the proposed method and outlines the direction of future research.

2. Materials and Methods

2.1. Related Work

Razavi introduced a small-signal model–based method for PSRR calculation [6]. This approach works well for simple and symmetric circuits by directly computing PSRR through the analysis of small-signal gain:

$$PSRR = \frac{A_{dm}}{A}, \tag{1}$$

where A_{dm} denotes the differential gain and A represents the overall gain of the small-signal model.

However, as circuit designs become more complex, especially with asymmetric or multistage circuits, the limitations of this method become evident. The extended method proposed by Grey [7] is theoretically more complete but suffers from cumbersome calculation procedures and unvalidated suitability for high-frequency circuits.

PSRR computation is influenced by the characteristics of the input, intermediate, and output stages of a two-stage operational amplifier. For instance, the bias current, input impedance, and offset voltage at the input stage significantly affect PSRR; circuits designed with low bias current and high input impedance tend to exhibit improved PSRR. In the intermediate stage, higher gain amplifies power supply noise, thereby reducing PSRR. Similarly, the output stage must be designed to balance driving capability with noise suppression to maintain a high PSRR.

To tackle the challenges associated with complex circuit analysis, we leverage Allen's interpretation of PSRR [8] and develop a "black-box" model that simplifies the intricate circuitry. This model is particularly applicable to Thevenin Equivalent Circuit Analysis, where the Thevenin theorem simplifies linear resistor networks with independent sources into a single voltage source in series with a resistance. Specifically, for any single-port network N, the port can be represented equivalently by a voltage source —whose value corresponds to the open-circuit voltage (V_o)—in series with a resistance R_o, which is the equivalent resistance observed at the port when all independent sources are deactivated.

 doi:10.20944/preprints202503.1187.v1

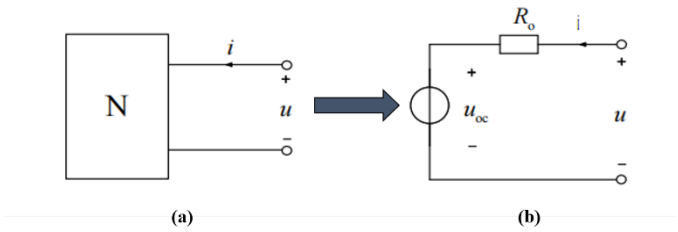


Figure 1. Thevenin equivalent circuit.

2.2. Proposed Methodology

In this section, we employ the black-box theory proposed in the previous chapter to analyze the PSRR of various operational amplifiers.

2.2.1. PSRR Calculation for P-Input Two-Stage Op-Amps

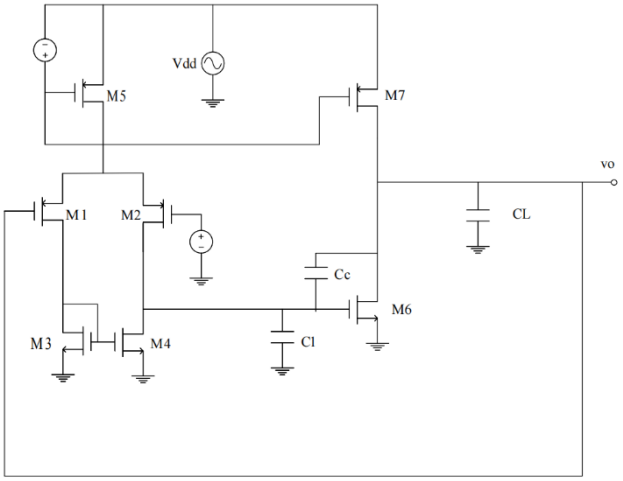


Figure 2. Typical structure of a P-input two-stage op-amp.

In this op-amp, the input stage usually consists of two P-type MOSFETs (M_1 and M_2) that receive the input signal and provide initial amplification. Transistors M_3 and M_4 act as load devices and work in conjunction with M_1 and M_2 to enhance the gain of the input stage. Current mirrors comprising M_5 and M_7 supply a stable bias current to the input stage while ensuring that the currents in M_1 and M_2 are matched. In the output stage, transistor M_6 further amplifies the signal from the input stage and provides sufficient drive capability for the load.

To simplify the calculation, we treat the first stage of the op-amp as a "black box" with input terminals which denoted as V_{in} and an output terminal which denoted as V_{out}. This is illustrated in Figure 3.

 doi:10.20944/preprints202503.1187.v1

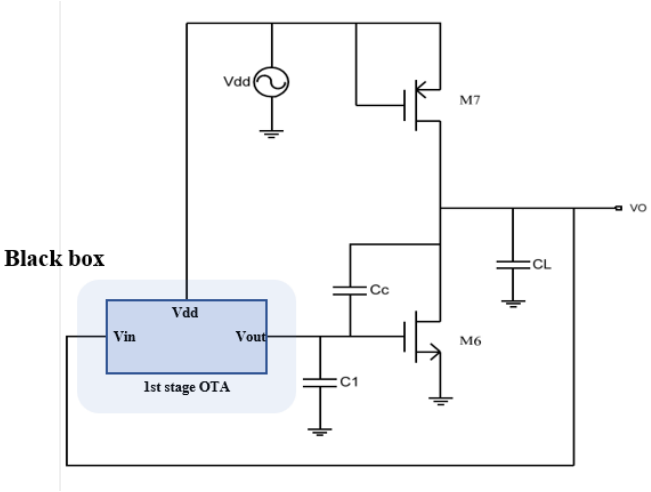


Figure 3. Two-stage op-amp circuit after "black-box" abstraction.

The processing of the first stage is performed in several steps:

(a) Evaluating the Impact of V_{dd} on the Thevenin Equivalent Output Voltage of the First Stage

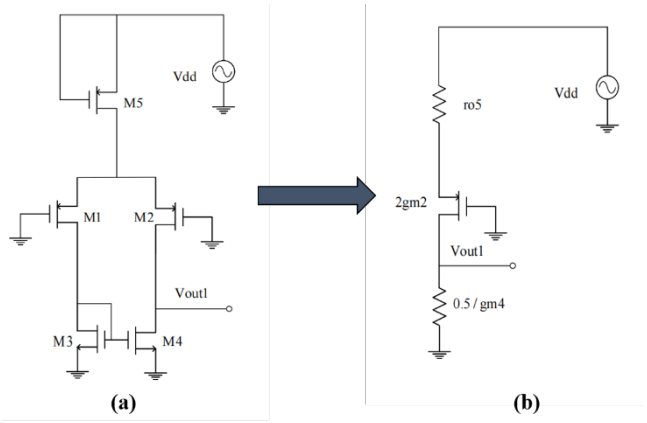


Figure 4. Thevenin equivalent circuit for the first stage of the op-amp.

The first stage is viewed as an independent module. Based on the Thevenin theorem, the equivalent voltage generated by V_{dd} is given by $V_{out1} = b_1 V_{dd}$.

$$b_1 \approx \frac{1}{2g_{m3}r_{o5}}, \tag{2}$$

(b) Evaluating the Impact of V_{in} on the Thevenin Equivalent Output Voltage of the First Stage

 doi:10.20944/preprints202503.1187.v1

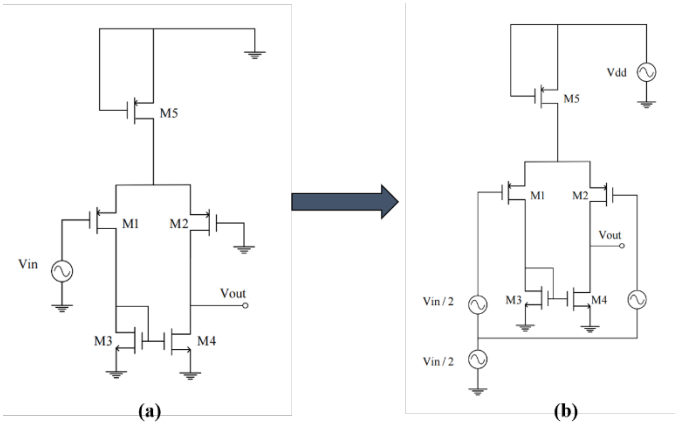


Figure 5. Thevenin equivalent output voltage of the first stage.

For a differential input V_{in} , the corresponding Thevenin equivalent output voltage is:

$$A = g_{m1}(r_{o2} \| r_{o4}), \tag{3}$$

Likewise, for a common-mode input V_{in}, the corresponding Thevenin equivalent output voltage is:

$$V_{th} = -\frac{V_{in}}{\frac{g_{m3}}{g_{m1}} + 2g_{m3}r_{o5}}, \tag{4}$$

The common-mode output voltage is relatively small and can be combined with the differential output voltage. Therefore, in the subsequent calculations, the common-mode contribution is typically neglected.

(c) Constructing the Thevenin Equivalent Circuit

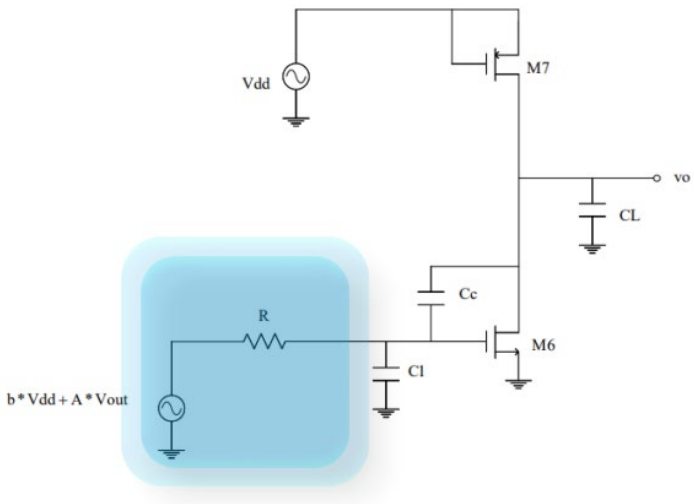


Figure 6. Thevenin equivalent circuit of the op-amp.

Using the superposition theorem, the first stage is further simplified to a structure consisting of a voltage source and a resistor, as shown in the lower left area of Figure 6, where $R = r_{o2} \| r_{o4}$ represents the output resistance of the first stage.

(a) Deriving the PSRR Transfer Function

 doi:10.20944/preprints202503.1187.v1

The equivalent circuit for the two-stage op-amp is shown in Figure 7. Considering the gate-drain capacitance C_{gd} of M_7, we use small-signal analysis to write the node current equations and thereby solve for the PSRR transfer function.

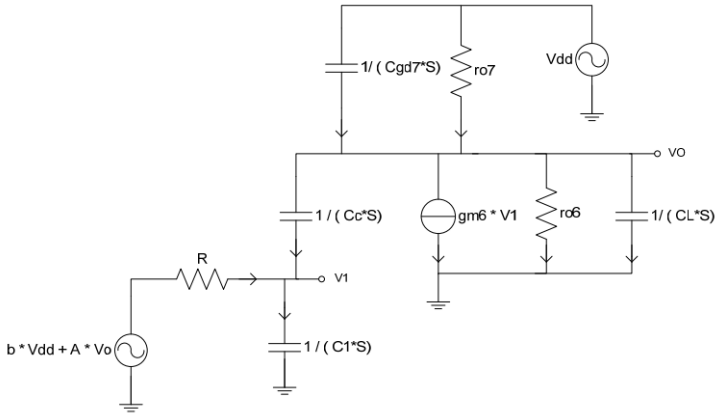


Figure 7. Small-signal equivalent model.

First, we write the node current equation at node V_1:

$$\frac{(b_1V_{dd}+AV_o)-V_1}{R}+s(V_o-V_1)C_c=V_1sC_1, \tag{5}$$

$$V_1=\frac{bV_{dd}+(A+RsC_c)V_o}{1+Rs(C_1+C_C)}, \tag{6}$$

Similarly, writing the node current equation at node V_o:

$$(V_o-V_1)sC_C+g_{m6}V_1+\frac{V_o}{r_{o6}}+V_osC_L=\frac{V_{dd}-V_o}{r_{o7}}+(V_{dd}-V_o)sC_{gd7}, \tag{7}$$

$$V_1=\frac{V_{dd}(\frac{1}{r_{o7}}+sC_{gd7})-V_o[(\frac{1}{r_{o7}}+\frac{1}{r_{o6}})+s(C_c+C_L+C_{gd7})]}{g_{m6}-sC_C}, \tag{8}$$

By equating (5) and (7):

$$V_1=\frac{V_{dd}(\frac{1}{r_{o7}}+sC_{gd7})-V_o[(\frac{1}{r_{o7}}+\frac{1}{r_{o6}})+s(C_c+C_L+C_{gd7})]}{g_{m6}-sC_C}=\frac{bV_{dd}+(A+RsC_c)V_o}{1+Rs(C_1+C_C)}, \tag{9}$$

$$\frac{1}{PSRR(s)}=\frac{V_o}{V_{dd}}, \tag{10}$$

In the derivation above, it is assumed that $L_5=L_7$, due to matching requirements. if we set $(\frac{W}{L})_7=M(\frac{W}{L})_5$ and $(\frac{W}{L})_6=N(\frac{W}{L})_3$, we obtain that $I_7=MI_5$, $r_{o5}=Mr_{o7}$, and:

$$\frac{g_{m6}r_{o7}}{2g_{m3}r_{o5}}=\frac{1}{2M}\sqrt{\frac{K_n'(\frac{W}{L})_6I_6}{K_n'(\frac{W}{L})_3I_3}}=\frac{1}{2M}\sqrt{\frac{(\frac{W}{L})_6}{(\frac{W}{L})_3}\times 2M}=\sqrt{\frac{N}{2M}}, \tag{11}$$

Next, we derive the DC PSRR value as well as the positions of the zero and pole:

 doi:10.20944/preprints202503.1187.v1

$$\frac{1}{|PSRR(s)|}=\frac{\frac{1}{r_{o7}}(1-\sqrt{\frac{N}{2M}})}{g_{m6}A+(\frac{1}{r_{o7}}+\frac{1}{r_{o6}})}\approx\frac{1-\sqrt{\frac{N}{2M}}}{Ag_{m6}r_{o7}}, \tag{12}$$

Assuming $Z_1 \ll Z_2, C_{gd7} \ll C_C, C_1 \ll C_C$, and for stability, we have $g_{m1} \ll g_{m6}$:

$$Z_1 \approx -\frac{\frac{1}{r_{o7}}(1-\sqrt{\frac{N}{2M}})}{\frac{R}{r_{o7}}(C_1+C_C)+C_{gd7}+b_1C_C}\approx-\frac{1-\sqrt{\frac{N}{2M}}}{R(C_1+C_C)+r_{o7}C_{gd7}}\approx-\frac{1-\sqrt{\frac{N}{2M}}}{R(C_1+C_C)}, \tag{13}$$

$$Z_2 \approx -\frac{\frac{R}{r_{o7}}(C_1+C_C)+C_{gd7}+b_1C_C}{RC_{gd7}(C_1+C_C)}\approx-\frac{R(C_1+C_C)+r_{o7}C_{gd7}}{r_{o7}RC_{gd7}(C_1+C_C)}\approx-\frac{1}{r_{o7}C_{gd7}}, \tag{14}$$

Further assuming $P_1 \ll P_2$, leads to:

$$P_1 \approx \frac{-[g_{m6}A+(\frac{1}{r_{o6}}+\frac{1}{r_{o7}})]}{(g_{m6}-g_{m1})RC_C+R(\frac{1}{r_{o6}}+\frac{1}{r_{o7}})(C_1+C_C)+(C_{gd7}+C_L+C_C)}\approx-\frac{g_{m6}A}{(g_{m6}-g_{m1})RC_C}\approx-\frac{g_{m6}g_{m1}}{(g_{m6}-g_{m1})RC_C}\approx-\frac{g_{m1}}{C_C}=\text{GB}$$

, (15)

$$P_2=\frac{g_{m6}}{C_1+C_L+C_{gd7}}, \tag{16}$$

$$\frac{1}{|PSRR(s)|}=\frac{1-\sqrt{\frac{N}{2M}}}{Ag_{m6}r_{o7}}\times\frac{(1+\frac{Rs(C_1+C_C)}{1-\sqrt{\frac{N}{2M}}})(1+r_{o7}C_{gd7})}{(1+\frac{s}{GB})(1+s\frac{C_1+C_L+C_{gd7}}{g_{m6}})}, \tag{17}$$

The location of Z_1 is the closest to the origin relative to the first pole. Whether the DC PSRR value is positive or negative depends on the specific values of N and M When N is approximately twice that of M, the DC PSRR value becomes very high; however, the zero also shifts closer to the origin.

The PSRR is influenced by two signal paths within the op-amp. In the first path, the signal entering from r_{o5} reduces the output voltage at low frequencies; in the second path, the signal entering from r_{o7} has the opposite effect and increases the output voltage. For simplification, the drain of M_5 is grounded, thereby neglecting the signal contribution from M_5 and resulting in a positive DC PSRR gain. Under ideal bias current source conditions, if N is greater than twice that of M, the PSRR is negative; if N is less than twice that of M, the PSRR is positive. The location of the zero is also closely related to the ratio of these two parameters.

PGB (PSR Gain Bandwidth):

By approximating the PSRR curve as having a single zero, and drawing an analogy with the gain-bandwidth product in op-amps, we define PGB as the product of the zero frequency and the DC PSRR value:

 doi:10.20944/preprints202503.1187.v1

$$PGB = | Z_1 \times PSRR | = | -\frac{1-\sqrt{\frac{N}{2M}}}{R(C_1+C_C)} \times \frac{Ag_{m6}r_{o7}}{1-\sqrt{\frac{N}{2M}}} | = \frac{g_{m1}g_{m6}r_{o7}}{C_1+C_C}, \quad (18)$$

According to (18), when the PGB value is large, the −20 dB/dec asymptote of the main zero shifts further away from the origin while maintaining its slope, thereby improving the frequency characteristics in the BE segment. If, while keeping other parameters constant, a parameter is adjusted so that it approaches 2M, the DC PSRR value increases significantly and the zero moves toward the origin, optimizing the frequency response in the C_L segment. If the frequency of interest falls on the DE segment of the curve, the impact of the parameter change is relatively small. As shown in Figure 8, curve CDE represents the original PSRR response, while curve ABE corresponds to the frequency response after a parameter adjustment.

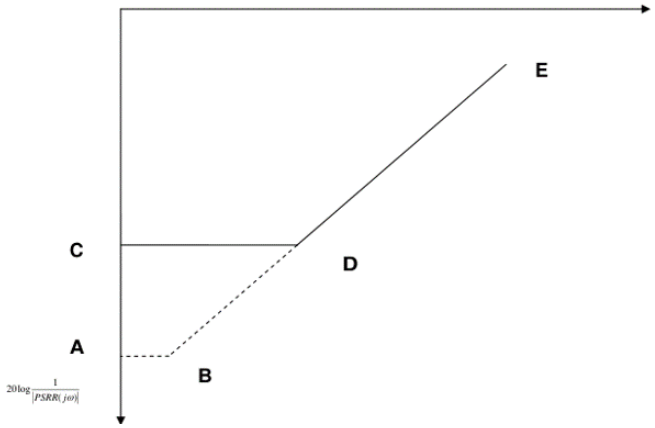


Figure 8. Impact of varying g_{m3} on the frequency characteristics of PSRR.

This process bears some similarity to considerations of the loop bandwidth (GB) of the two-stage op-amp. Increasing a particular parameter directly enhances the DC PSRR value, which is beneficial for our analysis. Under stability constraints, reducing the parameter C_c shifts ω_{-3dB} outward, thereby improving the frequency response; similarly, increasing g_{m6} shifts the BE line outward; increasing r_{o5} and r_{o7} directly optimizes the DC PSRR value; while increasing r_{o2} and r_{o4} raises the DC PSRR value but also moves ω_{-3dB} closer to the origin, benefiting only the low-frequency response—the PGB remains unchanged, and hence the improvement for high frequencies is limited. However, since the bandwidth that the industry is concerned about is usually low-frequency, PGB can play a vital role in the design of specific field.

2.2.1. PSRR Calculation for N-Input Two-Stage Op-Amps

In this subsection, we adopt a similar analytical approach to study the PSRR of N-input two-stage op-amps and thereby demonstrate the portability of the new PSRR calculation theory.

Based on the analysis in Section A for a typical P-input two-stage op-amp, we consolidate the simplified flowchart for a common N-input two-stage op-amp into a single diagram, as shown in Figure 9.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 March 2025 doi:10.20944/preprints202503.1187.v1

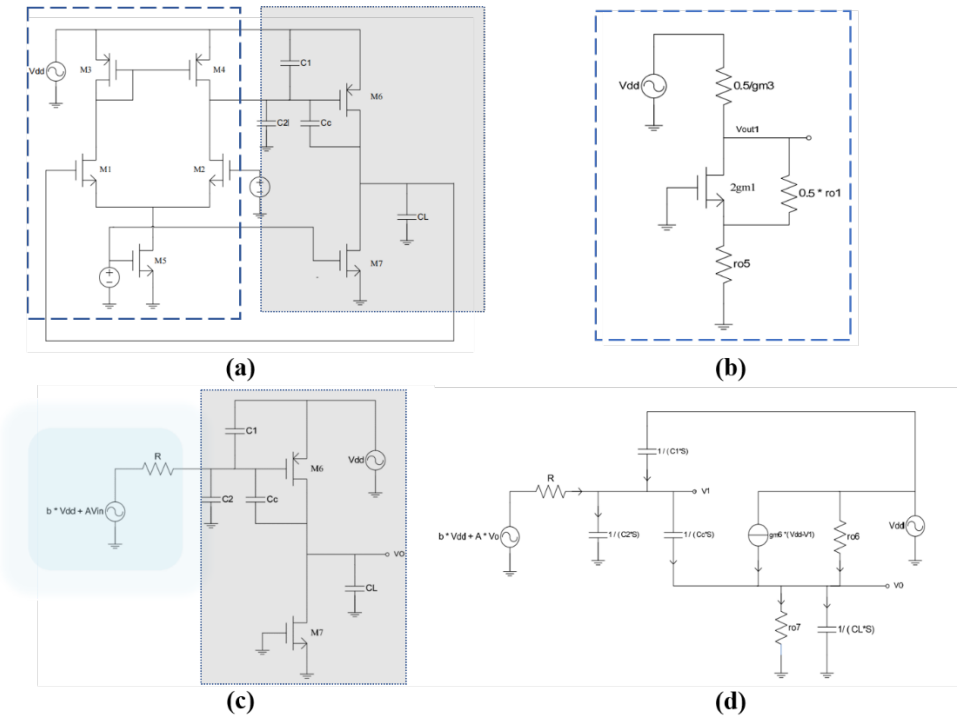


Figure 9. Simplified flow chart of a common N-input two-stage op amp.

The following quantities are computed: the Thevenin equivalent voltage due to V_{dd} from the first stage, the Thevenin equivalent voltage due to V_{in}, the PSRR, the DC PSRR value, the zero, the pole, and the PGB.

From Figure 9(b), the Thevenin equivalent voltage due to V_{dd} is given by $V_{out1} = b_2 V_{dd}$. While:

$$b_2 \approx \frac{g_{m1} r_{o1} r_{o5}}{\frac{1}{2g_{m3}} + g_{m1} r_{o1} r_{o5}} \approx \frac{2g_{m1} r_{o1} g_{m3} r_{o5}}{1 + 2g_{m1} r_{o1} g_{m3} r_{o5}} \approx 1, \tag{19}$$

Similarly, the Thevenin equivalent voltage due to V_{in} is AV_{in} :

$$A = g_{m1}(r_{o2} \parallel r_{o4}), \tag{20}$$

Using the node current equations, we obtain

$$V_1 = \frac{(b + RsC_1)V_{dd} + (A + RsC_C)V_o}{1 + Rs(C_1 + C_2 + C_C)}, \tag{21}$$

$$V_o \frac{V_{dd}(g_{m6} + \frac{1}{r_{o6}}) + V_o[(\frac{1}{r_{o6}} + \frac{1}{r_{o7}}) + s(C_C + C_L)]}{g_{m6} - sC_C}, \tag{22}$$

Equating (21) and (22) yields:

$$\begin{aligned} &V_o\{(g_{m6} - sC_C)(\mathrm{A} + RsC_C) + [(\frac{1}{r_{o6}} + \frac{1}{r_{o7}}) + s(C_C + C_L)][1 + Rs(C_1 + C_C + C_L)]\} \\ &= Vdd\{(g_{m6} + \frac{1}{r_{o6}})[1 + Rs(C_1 + C_C + C_L)] + (b_2 + RsC_1)(-g_{m6} + sC_C)\} \end{aligned}, \tag{23}$$

PSRR Calculation:

Under the assumptions that $Z_1 \ll Z_2$, $C_2 \ll C_C$, approximate expressions for the DC PSRR value and the zero can be derived as

 doi:10.20944/preprints202503.1187.v1

$$\frac{1}{|PSRR(s)|}=\frac{\frac{g_{m6}}{1+2g_{m1}r_{o1}g_{m3}r_{o5}}+\frac{1}{r_{o6}}}{Ag_{m6}+(\frac{1}{r_{o7}}+\frac{1}{r_{o6}})}\approx\frac{\frac{1}{r_{o6}}}{Ag_{m6}}=\frac{1}{Ag_{m6}r_{o6}}, \tag{24}$$

$$Z_1\approx-\frac{1}{g_{m6}r_{o6}R(C_2+C_C)}, \tag{25}$$

$$Z_2\approx-\frac{g_{m6}}{C_1}, \tag{26}$$

Assuming that $P_1\ll P_2$, $C_L\ll C_C$, $C_1\ll C_C$, $g_{m1}\ll g_{m6}$, he pole of the PSRR is approximately given by:

$$P_1\approx-\frac{g_{m6}}{C_C}=GB, \tag{27}$$

$$P_2\approx-\frac{g_{m6}}{C_1+C_2+C_L}=GB, \tag{28}$$

$$\frac{1}{PSRR(s)}=\frac{1}{Ag_{m6}r_{o6}}\times\frac{(1+g_{m6}r_{o6}Rs(C_2+C_C))(1+s\frac{C_1}{g_{m6}})}{(1+\frac{s}{GB})(1+s\frac{C_1+C_2+C_L}{g_{m6}})}, \tag{29}$$

Similarly, the calculation of PGB follows the same procedure as described previously.

$$PGB=|Z_1\times PSRR|=\frac{1}{g_{m6}r_{o6}R(C_2+C_L)}\times Ag_{m6}r_{o6}=\frac{g_{m1}}{C_2+C_L}, \tag{30}$$

From (30), it is apparent that the PGB of the N-input is relatively smaller. It is evident that by increasing the output resistance R of the first stage and the small-signal resistance R_{O6} of M_6, the DC PSRR value improves. However, the ω_{-3dB} point shifts closer to the origin, thereby enhancing only the low-frequency portion of the response, while the PGB remains unchanged. Under stability constraints, reducing C_C shifts ω_{-3dB} away from the origin and improves the frequency characteristics. Comparing the PGB values for the P-input and N-input two-stage op-amps (under ideal bias conditions), the frequency response of the P-input op-amp is superior by an order of magnitude.

2.2.1. P-Input Folded Cascode Op-Amps

The folded cascode structure is an efficient design for the op-amp input stage, significantly increasing the input impedance and gain while improving the power supply rejection. Following the approach used for the P- and N-input two-stage op-amps, we analyze the common P-input folded cascode op-amp structure and derive the relevant equations.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 March 2025 doi:10.20944/preprints202503.1187.v1

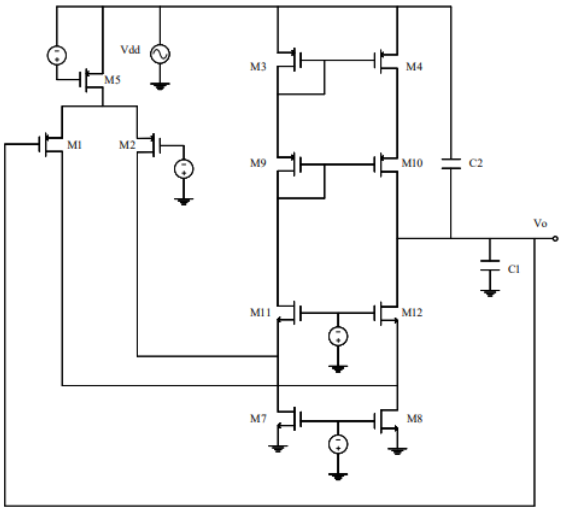


Figure 10. P-input folded cascode op-amp.

Using the Thevenin theorem, we first derive the open-circuit output voltage of the first stage. This open-circuit voltage can be computed by applying the superposition principle. The analytical approach is similar to that for the P- and N-input two-stage op-amps. First, the effect of the drain input signal from M_5 on the output is calculated. The circuit is modeled using the small-signal equivalent, and further simplified via Norton's theorem, as shown in Figure 11, yielding a Thevenin equivalent voltage of $V_{out1} = b_3 V_{dd}$, and:

$$b_3 \approx \frac{0.5(\frac{1}{g_{m3}} + \frac{1}{g_{m6}})}{0.5 r_{o5}} \approx (1 + \frac{g_{m3}}{g_{m6}}) \frac{1}{g_{m3} r_{o5}}, \tag{31}$$

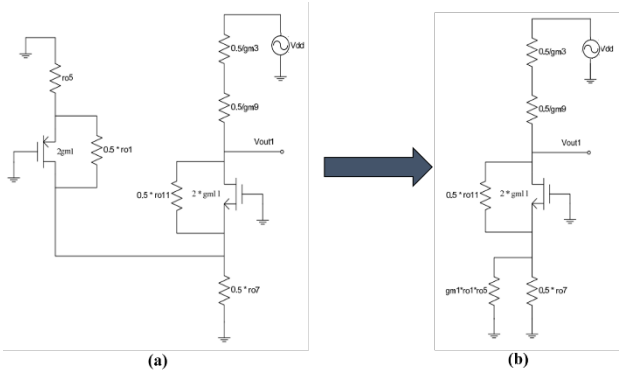


Figure 11. Equivalent circuit for the folded cascode op-amp.

Next, we calculate the effects of the drain input signals from M_3 and M_4 on the output. The resulting Thevenin equivalent voltage is $V_{out1} = m_1 V_{dd}$.

$$m_1 \approx \frac{g_{m11} r_{o11} \times (0.5 r_{o7}) \| (g_{m1} r_{o1} r_{o5})}{0.5(\frac{1}{g_{m3}} + \frac{1}{g_{m9}}) + g_{m11} r_{o11} \times (0.5 r_{o7}) \| (g_{m1} r_{o1} r_{o5})} \approx \frac{0.5 g_{m11} r_{o11} r_{o7}}{0.5(\frac{1}{g_{m3}} + \frac{1}{g_{m9}}) + 0.5 g_{m11} r_{o11} r_{o7}}$$
$$= \frac{g_{m3} g_{m11} r_{o11} r_{o7}}{g_{m3} g_{m11} r_{o11} r_{o7}} \tag{32}$$

,

 doi:10.20944/preprints202503.1187.v1

where it is found that $m_1 \approx 1$.

Subsequently, the effect of V_{in} on the output is computed; as shown in Figure 12, the Thevenin equivalent voltage induced by V_{in} is $-A\,V_{in}$ Finally, by applying the superposition theorem, the circuit is reduced to its simplest form:

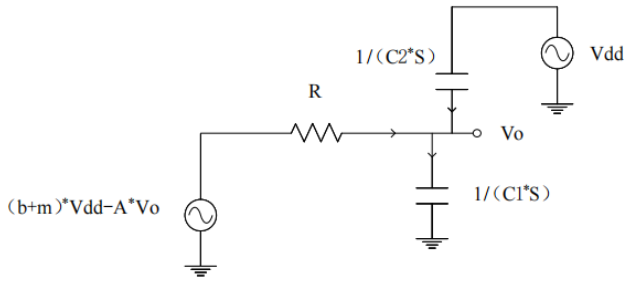


Figure 12. Folded cascode op-amp simplified using the superposition theorem.

$R = g_{m9}r_{o9}r_{o9} \parallel g_{m11}r_{o11}r_{o7}$ denotes the output resistance of the first stage. To calculate the PSRR, the values of V_o and V_{dd} must be determined. Based on the circuit diagram, we write the node current equation at V_o:

$$\frac{|(b_3+m_1)V_{dd} - AV_o| - V_o}{R} + (V_{dd} - V_o)sC_2 = V_o sC_1, \tag{33}$$

which simplifies to:

$$\frac{V_o}{V_{dd}} = \frac{(b_3+m_1)+RsC_2}{(A+1)+Rs(C_1+C_2)} \approx \frac{1+RsC_2}{A+Rs(C_1+C_2)}, \tag{34}$$

$\because b_3 + m_1 \approx 1$

$$\frac{1}{PSRR(s)} = \frac{V_o}{V_{dd}} \approx \frac{1}{A} \times \frac{1+RsC_2}{1+\frac{Rs(C_1+C_2)}{A}} = \frac{1}{A} \times \frac{1+RsC_2}{1+\frac{s(C_1+C_2)}{g_{m1}}}, \tag{35}$$

$$\frac{1}{|PSRR(s)|} = \frac{1}{A}, \tag{36}$$

$$Z = -\frac{1}{RC_2}, \tag{37}$$

$$P = -\frac{g_{m1}}{C_1+C_2}, \tag{38}$$

In this example, $R = g_{m9}r_{o9}r_{o9} \parallel g_{m11}r_{o11}r_{o7}$. The inverse of the DC PSRR value is equal to the op-amp gain. The PGB is then derived as:

$$PGB = |Z \times PSRR| = \frac{A}{RC_2} = \frac{g_{m1}}{C_2}, \tag{39}$$

Key design insights include:

(a) Increasing g_{m1} directly raises the DC PSRR value.

(b) Reducing the parasitic capacitance C_2 improves the frequency response.

(c) The dominant pole of the op-amp is associated with its output node. Consequently, augmenting C_1 shifts this pole closer to the origin, which is advantageous for enhancing both system stability

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 March 2025 doi:10.20944/preprints202503.1187.v1

and the frequency response of the PSRR. However, it is crucial to strike a balance with the required bandwidth; one cannot indiscriminately reduce the bandwidth without considering the overall system performance requirements.

2.2.1. N-Input Folded Cascode Op-Amps

Following the approach in Section 2.2.3, we analyze the N-input folded cascode op-amp. The simplified flowchart for a typical N-input two-stage op-amp is consolidated in Figure 13.

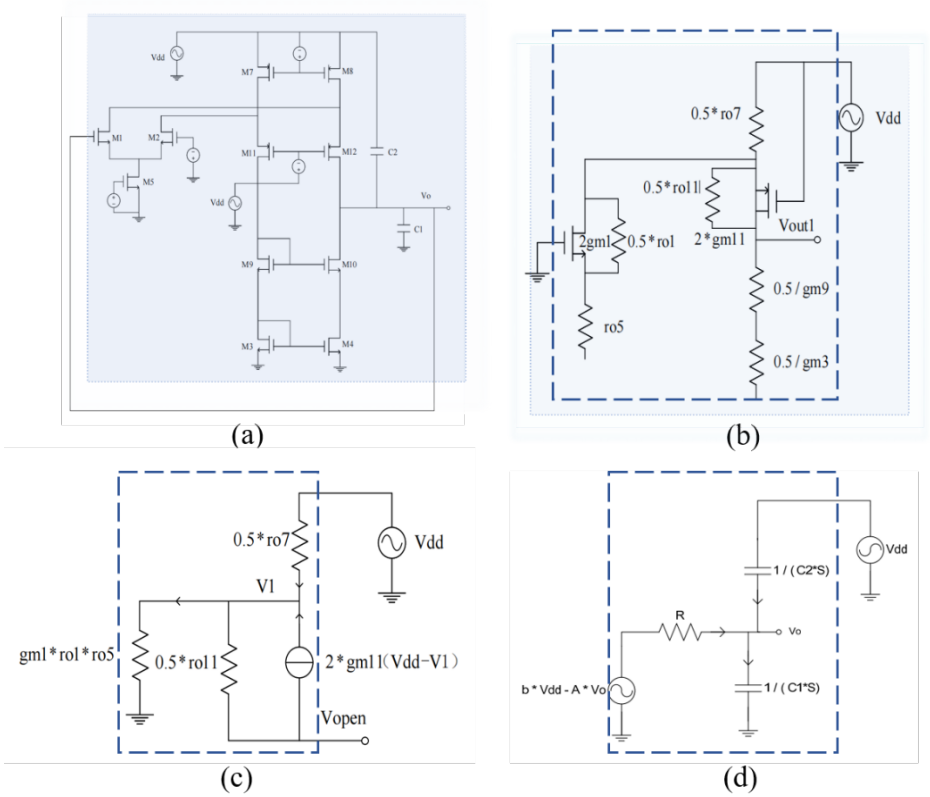


Figure 13. Simplified flowchart for a typical N-input two-stage op-amp.

From the Thevenin equivalent circuit, we obtain:

$$V_1 = V_{dd}\frac{g_{m1}r_{o1}r_{o5}}{0.5r_{o5}+g_{m1}r_{o1}r_{o5}}, \tag{40}$$

$$V_{dd}-V_1 = V_{dd}\frac{0.5r_{o5}}{0.5r_{o5}+g_{m1}r_{o1}r_{o5}}, \tag{41}$$

$$V_{open} = V_1 - 2g_{m11}(V_{dd}-V_1)\times 0.5r_{o11} = V_{dd}\frac{g_{m1}r_{o1}r_{o5}-g_{m11}r_{o11}r_{o7}}{0.5r_{o7}+g_{m1}r_{o1}r_{o5}} \approx V_{dd}(1-\frac{g_{m11}r_{o11}r_{o7}}{2g_{m1}r_{o1}r_{o5}}), \tag{42}$$

where the equivalent resistance is $R_{out} \approx 0.5g_{m11}r_{o11}r_{o7}$

Using resistive voltage division, the Thevenin equivalent voltage is found to be $V_{out1} = b_4 V_{dd}$ 。

$$b_4 \approx \frac{1+\frac{g_{m3}}{g_{m9}}}{g_{m11}r_{o11}g_{m3}r_{o7}}, \tag{43}$$

The Thevenin equivalent voltage induced by V_{in} is $-AV_{in}$:

 doi:10.20944/preprints202503.1187.v1

$$A = g_{m1}(g_{m9}r_{o9}r_{o7} \parallel g_{m11}r_{o11}r_{o7}), \tag{44}$$

Where $R = g_{m9}r_{o9}r_{o9} \parallel g_{m11}r_{o11}r_{o7}$ denotes the output resistance of the first stage. By writing the node current equation at node V_o, the relationship between V_{dd} and V_o is obtained:

$$V_{dd}(b + RsC_2) = V_o[(A+1) + Rs(C_1 + C_2)], \tag{45}$$

Subsequently, the PSRR is calculated as

$$\frac{1}{|PSRR(s)|} = \frac{1+\frac{g_{m3}}{g_{m9}}}{g_{m11}r_{o11}g_{m3}r_{o7}A}, \tag{46}$$

$$Z = -\frac{1+g_{m9}}{g_{m11}r_{o11}g_{m3}r_{o7}RC_2}, \tag{47}$$

$$P = -\frac{g_{m1}}{C_1 + C_2}, \tag{48}$$

C_1 is the compensation capacitor and C_2 represents the parasitic capacitance. Since the op-amp's input resistance R is very high, the zero is located near the origin, while the pole is far from the origin:

$$PGB = |Z \times PSRR| = -\frac{1+\frac{g_{m3}}{g_{m9}}}{g_{m11}r_{o11}g_{m3}r_{o7}RC_2} \times \frac{g_{m11}r_{o11}g_{m3}r_{o7}A}{1+\frac{g_{m3}}{g_{m9}}} = \frac{g_{m1}}{C_2}, \tag{49}$$

3. Results and Discussions

In this section, we will apply the proposed method to design a fully differential op amp with high PSRR. The circuit was designed using Cadence Virtuoso IC617 with a 180 nm CMOS process. We will first list the calculation process of several important indicators, and find the aspect ratio of each transistor through the constraints of multiple indicators. Then compare the simulation results with the calculation results to verify the accuracy of the PSRR calculation method

At the same time, we use the PGB formula to more intuitively know how to improve the PSRR of this complex circuit. We performed a simulation and verified the correctness of the PGB theory by comparing the PSRR before and after the modification.

At the end of this section, the simulation results of the circuit are given, and the expected indicators and the size of each transistor are given in a table at the end of the chapter for reference.

 doi:10.20944/preprints202503.1187.v1

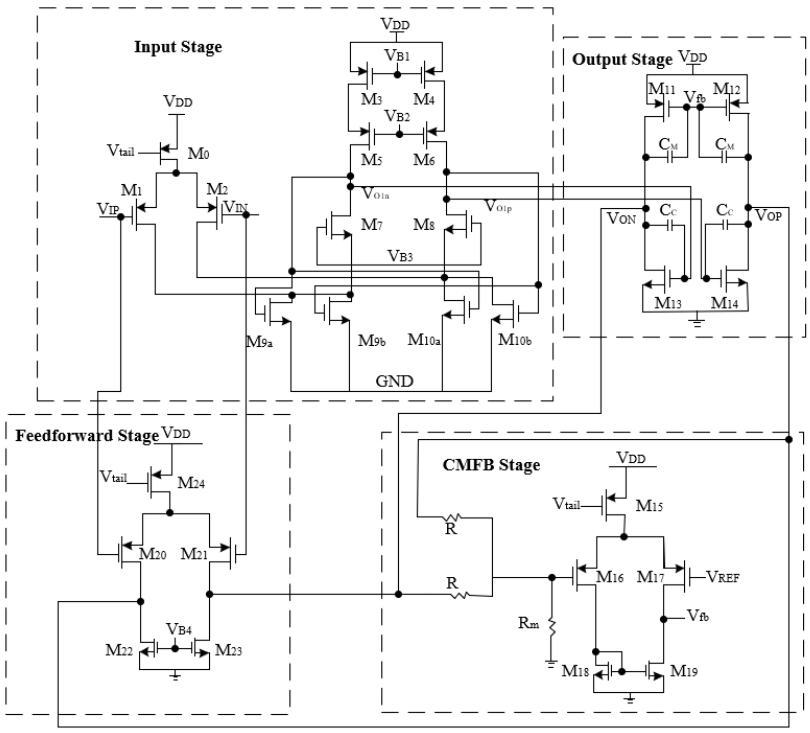


Figure 14. Circuit architecture.

(a). Gain Expression

The transconductance of the input stage, G_{m1}, is given as:

$$G_{m1} = g_{m1}, \tag{50}$$

The voltage gain is expressed as:

$$A_{v1} = -g_{m1}\{[g_{m7}r_{o7}(r_{o1} \| r_{o9a} \| r_{o9b})] \| (g_{m5}r_{o5}r_{o3})\}, \tag{51}$$

$$A_{v2} = -G_{m2}R_{o2} = -g_{m13}(r_{o11} \| r_{o13}), \tag{52}$$

$$A_{dm} = A_{v1} \bullet A_{v2}, \tag{53}$$

(b). Transfer Function Optimization

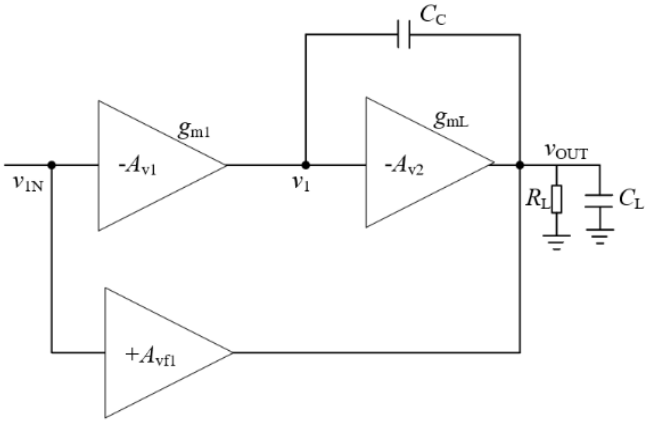


Figure 15. Equivalent block diagram.

 doi:10.20944/preprints202503.1187.v1

As illustrated in Figure 15, the feedforward stage introduces a zero-pole pair in the transfer function, compensating for the dominant pole. This minimizes phase lag and extends the high-frequency bandwidth. The transfer function is given by

$$A_v(s) = \frac{s[g_{mf1}(C_{o1} + C_C) - g_{m1}C_C] + g_{mf1}g_{o1} + g_{m1}g_{mL}}{s^2 d_2 + s d_1 + d_0}, \tag{54}$$

Where:

$d_2 = C_{o1}C_C + C_{out}(C_{o1} + C_C)$

$d_1 = g_{o1}C_{out} + g_{out}(C_{o1} + C_C) + (g_{o1} + g_{mL})C_C$

$d_0 = g_{o1}g_{out}$

$g_{o1} = \frac{1}{R_{o1}}$

(c). PSRR

We calculate the PSRR using the method presented in Chapter II. Referring to Figure 10. in Chapter II, the first stage of op amps can be equivalent to $V_{out} = (b_3 + m_1)V_{dd} + AV_{in}$, Where:

$$b_3 \approx (1 + \frac{g_{m3}}{g_{m6}})\frac{1}{g_{m3}r_{o0}}, \tag{55}$$

$$m_1 = \frac{g_{m3}g_{m11}r_{o7}(r_{o9a} \| r_{o9b})}{g_{m3}g_{m11}r_{o7}(r_{o9a} \| r_{o9b})} = 1, \tag{56}$$

Referring to the calculation in Figure 9., replace the original b with here and replace with the transfer function of PSRR that can be obtained directly

$$\frac{1}{PSRR(s)} = \frac{V_o}{V_{dd}}, \tag{57}$$

Assuming $Z_1 \ll Z_2$, $C_1 \ll C_C$, $C_1 = C_{gb14} + C_{db6} + C_{db8}$, $r_{o9}' = r_{o9a} \| r_{o9b}$, $C_{gd9}' = C_{gd9a} \| C_{gd9b}$

$$\frac{1}{|PSRR(s)|} = \frac{\frac{1}{r_{o6}} + [1 - (1 + \frac{g_{m14}}{g_{m5}})\frac{g_{m14}r_{o14}}{g_{m3}r_{o14}}}{g_{m14}A + (\frac{1}{r_{o14}} + \frac{1}{r_{o12}})} \approx \frac{1 - (1 + \frac{g_{m3}}{g_{m5}})\frac{g_{m14}r_{o14}}{g_{m5} - g_{m3}r_{oo}}}{g_{m14}r_{o14}A} \tag{58}$$

$$Z_1 = -\frac{\frac{1}{r_{o14}} + [1 - (1 + \frac{g_{m3}}{g_{m5}})\frac{g_{m14}r_{o14}}{g_{m3}r_{oo}}}{R(g_{m14} + \frac{1}{r_{o14}})(C_{gs14} + C_1 + C_C) + (b_3C_C - g_{m14}RC_{gs14})} \approx -\frac{1 - (1 + \frac{g_{m3}}{g_m})\frac{g_{m14}r_{o14}}{g_{m3}r_{oo}}}{g_{m14}r_{o14}R(C_1 + C_C)}, \tag{59}$$

$$Z_2 = -\frac{R(g_{m14} + \frac{1}{r_{o14}})(C_{gs14} + C_1 + C_C) + (b_3C_C - g_{m14}RC_{gs14})}{RC_{gs14}C_C} \approx -\frac{g_{m14}R(C_1 + C_C)}{RC_{gs14}C_C} \approx -\frac{g_{m14}}{C_{gs14}} \tag{60}$$

If $P_1 \ll P_2$, $C_1 \ll C_C$, $C_L \ll C_C$:

$$P_1 \approx \frac{-[g_{m14}A + (\frac{1}{r_{o14}} + \frac{1}{r_{o9}})]}{(g_{m14} - g_{m1})RC_C + R(\frac{1}{r_{o14}} + \frac{1}{r_{o9}'})(C_{gd14} + C_C) + (C_{gd9}' + C_L + C_C)} \approx -\frac{g_{m14}A}{(g_{m14} - g_{m1})RC_C} \approx -\frac{g_{m14}g_{m1}}{(g_{m14} - g_{m1})RC_C} \approx -\frac{g_{m1}}{C_C} = \text{GB}$$

, (61)

 doi:10.20944/preprints202503.1187.v1

$$P_2 = -\frac{g_{m6}}{C_{gs14} + C_L + (C_{gd9a} \parallel C_{gd9b})}, \tag{62}$$

$$\frac{1}{PSRR(s)} = \frac{1-(1+\frac{g_{m3}}{g_{m2}})\frac{g_{m14}r_{o14}}{g_{m3}r_{o0}}}{g_{m14}r_{o14}A} \times \frac{(1+\frac{g_{m14}r_{o14}(C_1+C_C)s}{g_{m6}r_{o6}})(1+\frac{C_{gs14}}{g_{m14}}s)}{(1+\frac{s}{GB})(1+\frac{C_{gs14}+C_1+C_C}{g_{m14}}s)}, \tag{63}$$

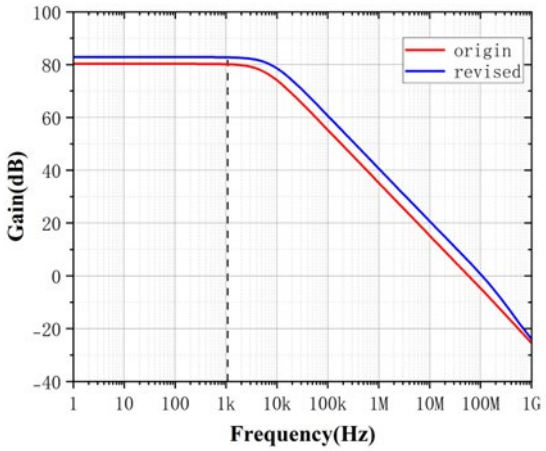
$$PGB = |Z_1 \times PSRR| = |\frac{1-(1+\frac{g_{m3}}{g_{m5}})\frac{g_{m14}r_{o14}}{g_{m5}}}{g_{m14}r_{o14}R(C_1+C_C)} \times \frac{g_{m14}r_{o14}A}{1-(1+\frac{g_{m3}}{g_{m5}})\frac{g_{m14}r_{o14}}{g_{m3}r_{o0}}}| = \frac{g_{m1}}{C_1+C_C}, \tag{64}$$

Constrained by the above formula, we can easily find the size of each transistor. Table 1 shows the design specifications of this circuit.

Table 1. The design specifications of this circuit.

Parameters	
Supply Volatge（V）	1.8V
Process	180nm
Gain（dB）	>80dB
Phase Margin（deg）	>55
GBW(MHz)	>100
SR（V/us）	>80
Power(mW)	<1
CMRR（dB）	-
PSRR(dB)	>100
C_L(F)	2p
FOM*	-

And after simulation, we hope to further optimize the performance of PSRR. Compared with the traditional analysis of PSR in the industrial method, we know more intuitively that we can enhance the performance of PSRR by increasing gm or reducing cc according to (64). The simulation results before and after the modification are shown below:



 doi:10.20944/preprints202503.1187.v1

Figure 16. Gain simulation experiment.

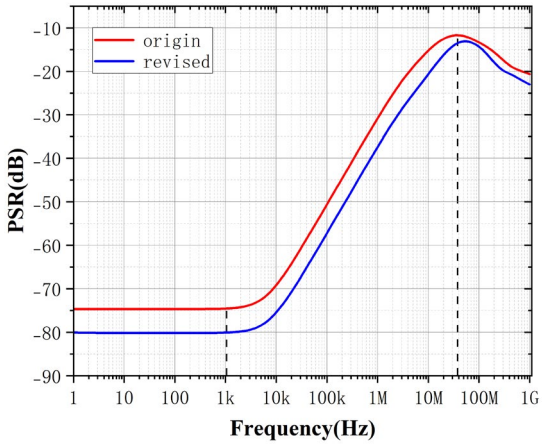


Figure 17. PSR simulation experiment.

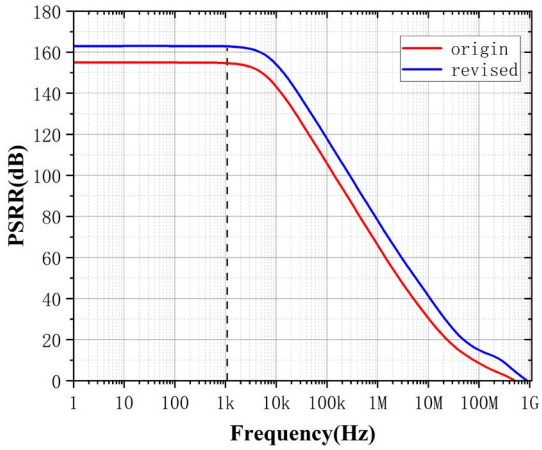


Figure 18. PSRR simulation experiment.

As shown in the above, the modified circuit has improved DC gain performance due to the increase in the width of the input transistor. In addition, the performance of PSR and PSRR is even better, which verifies the ability of PGB to help analog circuit designers improve PSRR more intuitively in complex circuits.

We also performed some other simulations on the circuit. Figure 19 shows the basic indicators of the circuit at different process corners, and Figure 19-d shows the PSRR of the circuit at each process corner after PGB operation adjustment

 doi:10.20944/preprints202503.1187.v1

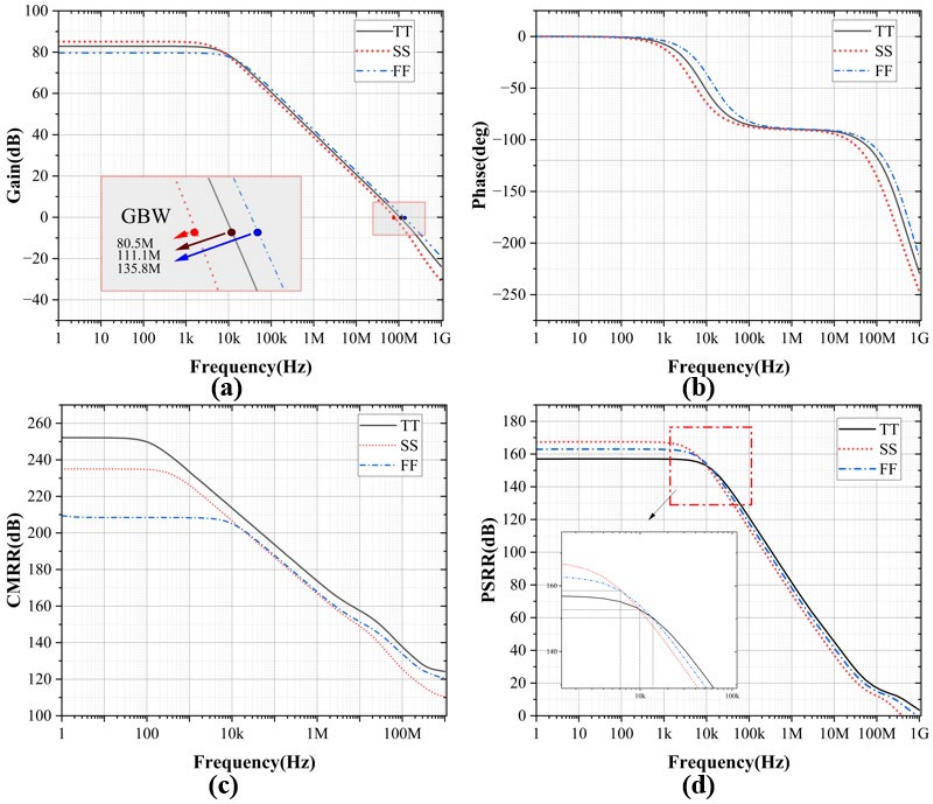


Figure 19. Simulation results at different process conners of the proposed OTA (a) The AC Gain (b) Phase (c)CMRR (d) PSRR.

The PSRR of this circuit is more than 100dB at 100kHz for all process conners. It is also very good at high frequencies. We also did a Monte Carlo simulation, and the results are shown in the Figure 20.

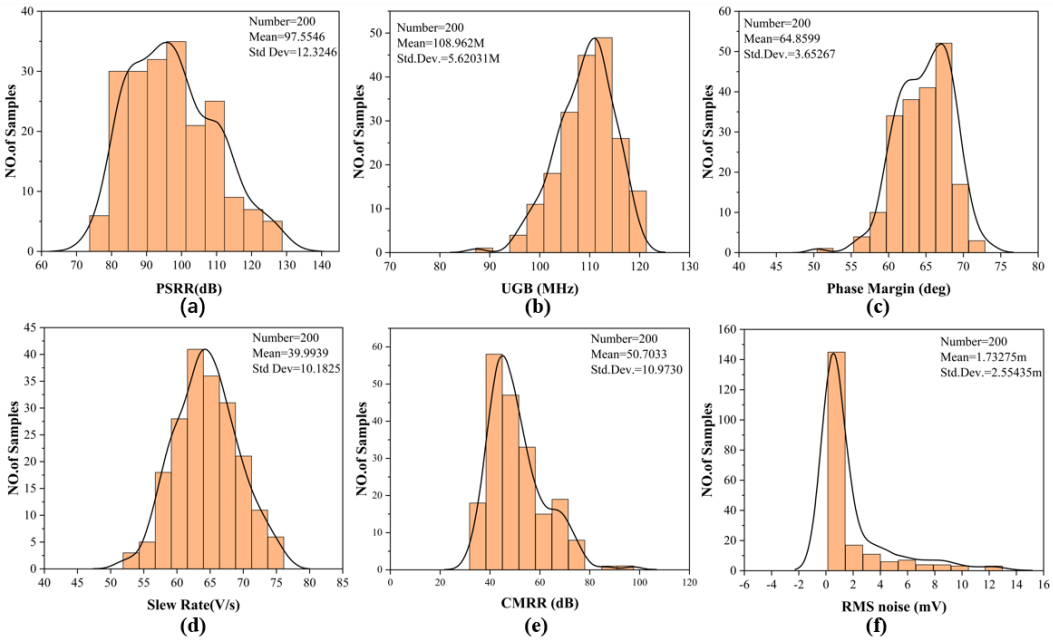


Figure 20. Monte Carlo simulation of (a) PSRR (b) Unity gain bandwidth (c) Phase margin (d) Slew Rate (e) CMRR (f) RMS noise.

 doi:10.20944/preprints202503.1187.v1

Table 2. Performance of the implemented OTA in comparison to the existing works.

Parameters	Designed	This Work	8	9	10	11
Supply Voltage (V)	1.8V	1.8V	1.8V	1.8V	2V	1.2V
Process	180nm	180nm	180nm	180nm	45nm	65nm
Gain (dB)	>80dB	83dB	67dB	66dB	141	90.17
Phase Margin (deg)	>55	61.4	54	58.5	60	88.84
GBW (MHz)	<100	111.1	111.8	60	101	1410
SR (V/us)	>80	100	32.30	95	57.7	-
Power (mW)	<1	0.95	1.37	0.55	1.2	47.25
CMRR (dB)	-	252		127	136	-
PSRR (dB)	>100	131	68	83.2	57/67	-
C_L (F)	2p	2p	2p	2.3p	1p	4p
FOM*	-	233.8	163.2	240	80	119.3

$$FOM = \frac{GBW \times C_L}{TotalPower}$$

Table 2 shows the simulation results of this circuit and the comparison with other high PSRR op amps. Table 3 shows the comparison between the expected performance and simulation results of the circuit designed using our proposed PSRR calculation method. The design requirements are achieved in all indicators and a good FOM value is achieved. The PSRR calculation method proposed in this article provides a new idea for future circuit design, and the PGB optimization method can also simplify the complex process of PSR calculation.

Table 3. Sizes obtained from the multiple constraints.

Components	W/L(um)
M0	9.9/1
M1 M2	123/1
M3 M4	32/3
M5 M6	15/1
M7 M8	10/0.6
M9a M9b M10a M10b	2.05/0.945
M11 M12	30/1
M13 M14	4.9/3.5
M15	10/1
M16 M17 M20 M21	6/0.18
M18 M19	1/1
M22 M23	1/4
M25	12/1

4. Conclusions

Experimental validation in Section III demonstrates that by leveraging Thevenin's equivalence principle, the proposed method transforms multi-stage op-amps into simplified black-box models,

 doi:10.20944/preprints202503.1187.v1

significantly reducing computational complexity while enhancing intuitive analysis. The introduced PGB metric, which correlates the DC PSRR value with the first dominant pole frequency, eliminates the reliance on exhaustive S-parameter modeling. This enables a computationally efficient evaluation of PSRR performance within the target frequency band. While the PGB framework assumes validity primarily below the GBW—a constraint inherent to its first-order approximation—it remains highly practical for industrial design scenarios where critical PSRR specifications typically reside in low-to-mid frequency ranges. the PGB metric provides actionable insights for optimizing PSRR through parameter adjustments and facilitates rapid comparative analysis of competing circuit topologies.

The proposed framework not only simplifies PSRR analysis for asymmetric and multi-stage circuits but also provides actionable insights for optimizing key parameters (e.g., transconductance, compensation capacitance) to meet stringent industrial requirements. Future work will extend this approach to mixed-signal systems and explore its integration with machine learning-driven design automation tools.

Author Contributions: Conceptualization, Yi Zhang.; methodology, Yi Zhang; software, Yi Zhang; validation, Yi Zhang; formal analysis, Yi Zhang and Ruonan Lin; investigation, Xin Yang and Ruonan Lin; resources, Tailai Li; data curation, Yi Zhang.; writing—original draft preparation, Xin Yang; writing—review and editing, Tailai Li; visualization, Yi Zhang and Xin Yang; supervision, Yi Zhang; project administration, Yi Zhang; All authors have read and agreed to the published version of the manuscript."

Funding: This research received no external funding.

Data Availability Statement: All data for this article are available

Acknowledgments: None.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. J. S. Kim, S. Ha, H. Jeong and J. Roh, "A High-PSRR NMOS LDO Regulator With Intrinsic Gain-Tracking Ripple Cancellation Technique," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 71, no. 11, pp. 4951-4960, Nov. 2024, doi:10.1109/TCSI.2024.3422001.
2. A. I. Colli-Menchi, J. Torres and E. Sánchez-Sinencio, "A Feed-Forward Power-Supply Noise Cancellation Technique for Single-Ended Class-D Audio Amplifiers," in IEEE Journal of Solid-State Circuits, vol. 49, no. 3, pp. 718-728, March 2014, doi: 10.1109/JSSC.2014.2298456.
3. C. -C. Chiu et al., "A 0.6 V Resistance-Locked Loop Embedded Digital Low Dropout Regulator in 40 nm CMOS With 80.5% Power Supply Rejection Improvement," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, no. 1, pp. 59-69, Jan. 2015, doi: 10.1109/TCSI.2014.2342380.
4. Y. Choi, W. Tak, Y. Yoon, J. Roh, S. Kwon and J. Koh, "A 0.018% THD+N, 88-dB PSRR PWM Class-D Amplifier for Direct Battery Hookup," in IEEE Journal of Solid-State Circuits, vol. 47, no. 2, pp. 454-463, Feb. 2012, doi: 10.1109/JSSC.2011.2170770.
5. K. A. I. Halonen, W. M. C. Sansen and M. Steyaert, "A micropower fourth-order elliptical switched-capacitor low-pass filter," in IEEE Journal of Solid-State Circuits, vol. 22, no. 2, pp. 164-173, April 1987, doi: 10.1109/JSSC.1987.1052698.
6. B. Razavi, "Design of Analog CMOS Integrated Circuits," 2nd ed., Xi'an Jiaotong University Press, 2009, pp. 358–400
7. P. E. Allen, D. R. Holberg, "CMOS Analog Circuit Design," 2nd ed., Beijing: Publishing House of Electronics Industry, 2005, pp. 232–234
8. P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 4th ed., Beijing: Higher Education Press, 2005, pp. 410–415.

 doi:10.20944/preprints202503.1187.v1

9. Bhar S, Mondal A, Srimani S, et al. A low power driver amplifier for Fully Differential ADC[C]//2019 2nd International Symposium on Devices, Circuits and Systems (ISDCS). IEEE, 2019: 1-6
10. E. Yang and T. Lehmann, ''High gain operational amplifiers in 22 nm CMOS,'' in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2019, pp. 1–5.
11. S. Chakraborty, A. Pandey, and V. Nath, ''Ultra high gain CMOS op-amp design using self-cascoding and positive feedback,'' Microsyst. Technol., vol. 23, no. 3, pp. 541–552, Mar. 2017.
12. Yongzhen Chen, Chixiao Chen, Qiang Zhang, Fan Ye and Junyan Ren, "A 12-bit 200-MS/s sample-and-hold amplifier with a hybrid Miller-Feedforward compensation technique," 2013 IEEE 10th International Conference on ASIC, 2013, pp. 1-4, doi:10.1109/ASICON.2013.6811866.