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A Family of Five-Level Pseudo-Totem Pole Dual Boost Converters

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Abstract: In this paper, based on the pseudo-totem pole (PTP) circuit, a family of five-level PTP dual boost converters (PDBC) is proposed. Dual boost converter has some unique advantages such as no bridge arm shoot-through risk and no switch body diode reverse recovery problem, so that it has a good application prospect. Compared with conventional three-level PTP converters, PDBCs has higher power density, higher efficiency, and low voltage and current stress. The topological derivation process, working principle, modulation and strategy of the topology are analyzed firstly. Further, the number of power devices, the switches voltage and current stress of the proposed topology is analyzed. Finally, a representative five-level PDBC experimental prototype is designed with AC input 220V/50Hz, DC output 400V/1kW, and peak efficiency of 98.27%. The experimental results show that the five-level PDBC proposed in this paper has higher efficiency and verify the correctness of the topology.

Keywords: five-level dual boost converter; pseudo-totem pole (PTP); efficiency; voltage and current stress

1. Introduction

With the development of power electronics technology, the neutral point clamped (NPC) multi-level converter has attracted more and more scholars' attention [1-2]. Multi-level NPC converters has the advantages of high efficiency, high power density, low total harmonic distortion (THD), low voltage and current stress [3-5]. Therefore, multi-level NPC converters are widely used in medium and high power, medium voltage applications [6-9], such as electric vehicles (EVs), motor drives, electrical railway traction, and DC-bus microgrids [10-13].

Compared with IGBT, power MOSFET has some excellent characteristics such as high frequency operation, low switching loss, and low conduction loss. Therefore, power MOSFET is widely used in low-power converters to improve efficiency and reduce the volume. However, due to the poor reverse recovery characteristics of body diode, MOSFET-based have a risk of device failure, which is related to the phase-leg shoot, may cause false triggering of the gate voltage. Therefore, conventional H-bridge converters often used IGBTs [14-17]. The dual boost/buck converter can avoid the shoot-through problem effectively, and the freewheeling current flows through the independent diode to solve the MOSFET body diode reverse recovery problem [14-21]. However, due to the two inductance structure of the dual boost/buck converter, the volume and weight of the converter will increase. In this regard, in [16, 17, 22], the multi-level dual boost/buck converter is proposed to reduce the size and weight of this type of topology.

The bridgeless converter has high power factor (PF), low THD, and high efficiency. It usually includes the basic bridgeless converters, the bidirectional-switch bridgeless converters, the totem pole bridgeless converters, and the PTP bridgeless converters [22-24]. Among them, the PTP bridgeless converter has a simple structure, few semiconductor devices conducting in the series loop, and a natural dual boost structure. In order to increase the power density and reduce the THD, the PTP bridgeless converter must work at a higher frequency. Moreover, all the active devices in the circuit bear the DC voltage, which cause the high voltage stress [3].

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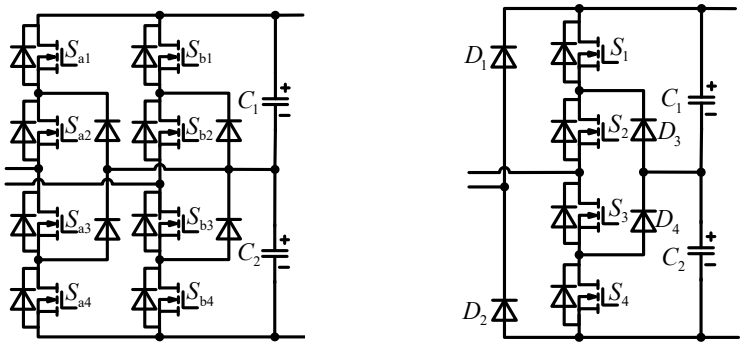
Figure 1 shows two common five-level converter topologies. Figure 1a is conventional five-level converter (CFLC), which is widely used in bidirectional power flow scenario such as vehicle to gird (V2G). However, the number of switch is large, which can be further optimized for reduce the number of switch. Figure 1b is unidirectional five-level converter proposed in [25], which using only one NPC bridge arm in CFLC to reduce the number of switch. However, there is less topology derivation process. In [4], a new five-level converter with high power density is proposed and the current stress is analyzed, however, the number of active devices is large, and the cost is high. In [14, 16], the PTP bridgeless structure is adopted to achieve five-level dual buck grid-connected inverter, and summarizes a topology structure method to expand the circuit. However, the utilization of two input inductors is low.



(**a**) (**b**)

Figure 1. The common five-level converter topologies. (**a**) Conventional five-level converter; (**b**) Converter proposed in [25].

Based on the above analysis, the bridge arm of the topology proposed in [25] is used as the prototype to obtain new five-level bridge arms. By cascading five-level bridge arms with the three-level PTP circuit, a family of five-level PDBCs is proposed. The proposed PDBC optimizes the three-level PTP converter in terms of large volume and large switching loss, and retaining the dual boost structure, which have advantages of high reliability.

The structure of this paper is as follows. Section 2 derives the PDBC in detail and analyzes the working principle. Section 3 designs the control and modulation strategy of PDBC. In section 4, the voltage and current stress are analyzed. Section 5 conducts experimental verification on PDBC. Finally, section 6 concludes the paper.

2. Topological Derivation and Operating Principle

2.1. Topological Derivation

Figure 2 shows the three most commonly used clamping bridge arm structures in five-level converters. A new five-level converter can be obtained by cascading these three clamping bridge arm structures with a three-level circuit.

In this paper, the bridge arm shown in Figure 2b is used to generate a new bridge arm, as shown in Figure 3. For ease of description, the bridge arms are numbered below each bridge arms i.e. A1, A2. Firstly, the two diodes on the right side of A4 are replaced with MOSFETs to get A1*. Then removed S_2 and S_4 of A1*, and reconnected them to get a new bridge arm A2, as shown in Figure 3a. In the same way, remove S_1 and S_3 of A1*, and then reconnect them to obtain a new bridge arm A3, as shown in Figure 3b.

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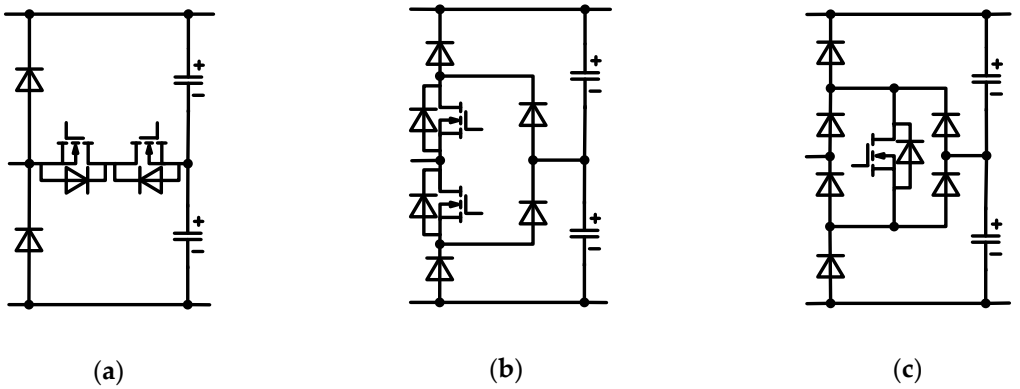
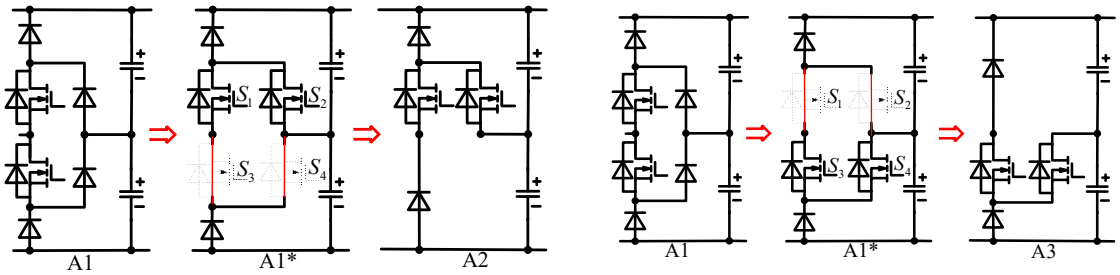


(a) (b) (c)

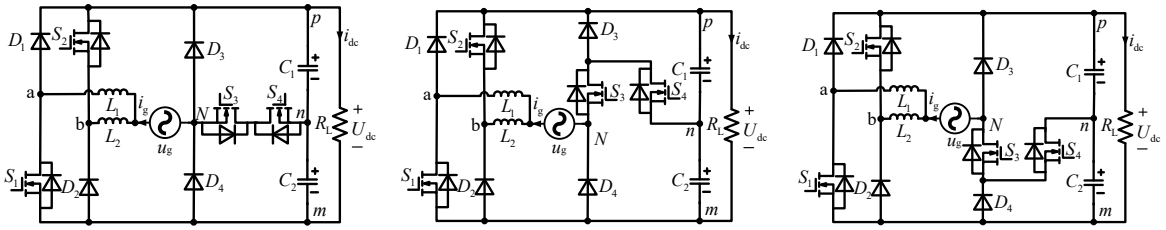
Figure 2. Three most commonly used clamping bridge arm structures. (**a**) T-type three-level bridge arm structure; (**b**) Diode Neutral Point Clamping (DNPC) three-level bridge arm structure; (**c**) Single switch three-level bridge arm structure.



(a) (b)

Figure 3. Topology derivation. (**a**) Topology derivation of A2; (**b**) Topology derivation of A3.

Through the bridge arm transformation in Figure 3, new bridge arms A2 and A3 are derived. Figure 4 shows a family of five-level PTP dual boost converters, which named as PDBC-I, PDBC-II and PDBC-III, respectively. It can be seen in Figure 4, the PTP dual boost converter is cascaded with Figure 2(a), A2, and A3 to generate the PDBCs, respectively.



(a) (b) (c)

Figure 4. A family of five-level PTP dual boost converters. (**a**) PDBC-I; (**b**) PDBC-II; (**c**) PDBC-III.

Compared with the traditional five-level converter, a family of PDBCs proposed in this paper reduces the number of MOSFETs by four, so it can effectively reduce the converter loss. It is worth mentioning that the three power flow converters proposed in this paper can all achieve bidirectional power flow after a slight circuit modification.

2.2. Operating Principle

Based on the above analysis, this paper takes the PDBC-II as an example for working mode analysis. Figure 5 shows the key waveforms of one power cycle, which are corresponding to the six working modes in Figure 6. For ease of analysis, it is assumed that the circuit works in continuous conduction mode (CCM), the inductances and capacitors are large enough, the capacitor voltage

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$U_{C1}=U_{C2}=U_{dc}/2$, and the DC voltage U_{dc} is remain constant. Figure 6 shows the six working modes of PDBC-II, which are corresponding to 0, ±0.5U_{dc} and ±U_{dc}, respectively. The six working modes are analyzed as follows.

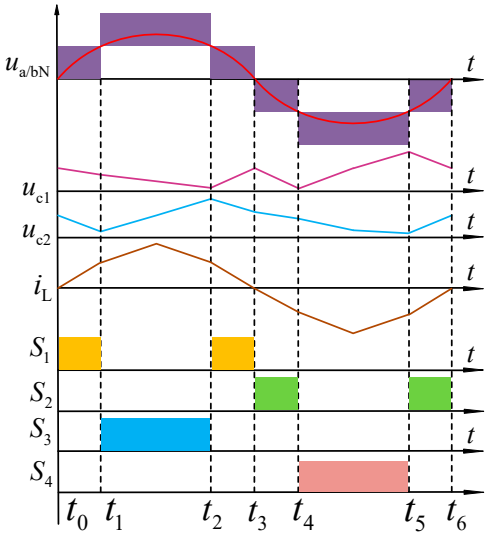

Figure 5. Key waveforms of six working modes in one cycle.

Working mode 1: During [t_0, t_1] shown in Figure 5, the grid voltage u_g>0, u_{aN}=0, u_{bN}=u_g. In this mode, the current path is shown in Figure 6a. As shown in Figure 6a, the switch S_1 is ON, the diode D_4 is ON, and the other active components are OFF. The capacitors C_1 and C_2 are discharging to the load R_L.

Working mode 2: During [t_1, t_2] shown in Figure 5, the grid voltage u_g>0, u_{aN}=u_{bN}=$U_{dc}/2$. In this mode, the current path is shown in Figure 6b. As shown in Figure 6b, the switch S_3 is ON, the body diodes of S_2 and S_4 are ON, the diode D_1 is ON, and the other active components are OFF. The capacitor C_1 is charging and C_2 is discharging to the load R_L.

Working mode 3: During [t_2, t_3] shown in Figure 5, the grid voltage u_g>0, u_{aN}=u_{bN}=U_{dc}. In this mode, the current path is shown in Figure 6c. As shown in Figure 6c, the body diode of S_2 is ON, the diodes D_1 and D_4 are ON, and the other active components are OFF. The capacitors C_1 and C_2 are charging, and the AC power supplies to the load R_L.

Working mode 4: During [t_3, t_4] shown in Figure 5, the grid voltage u_g<0, u_{bN}=u_g, u_{bN}=0. In this mode, the current path is shown in Figure 6d. As shown in Figure 6d, the switch S_2 is ON, the body diode of S_3 is ON, the diode D_3 is ON, and the other active components are OFF. The capacitors C_1 and C_2 are discharging to the load R_L.

Working mode 5: During [t_4, t_5] shown in Figure 5, the grid voltage u_g<0, u_{aN}=u_{bN}=−$U_{dc}/2$. In this mode, the current path is shown in Figure 6e. As shown in Figure 6e, the switch S_4 is ON, the body diodes of S_1 and S_3 are ON, the diode D_2 is ON, and the other active components are OFF. The capacitor C_2 is charging and C_1 is discharging to the load R_L.

Working mode 6: During [t_5, t_6] shown in Figure 5, the grid voltage u_g<0, u_{aN}=u_{bN}=−U_{dc}. In this mode, the current path is shown in Figure 6f. As shown in Figure 6f, the body diodes of S_1 and S_3 are ON, the diodes D_2 and D_3 are ON, and the other active components are OFF. The capacitors C_1 and C_2 are charging, and the AC power supplies to the load R_L.

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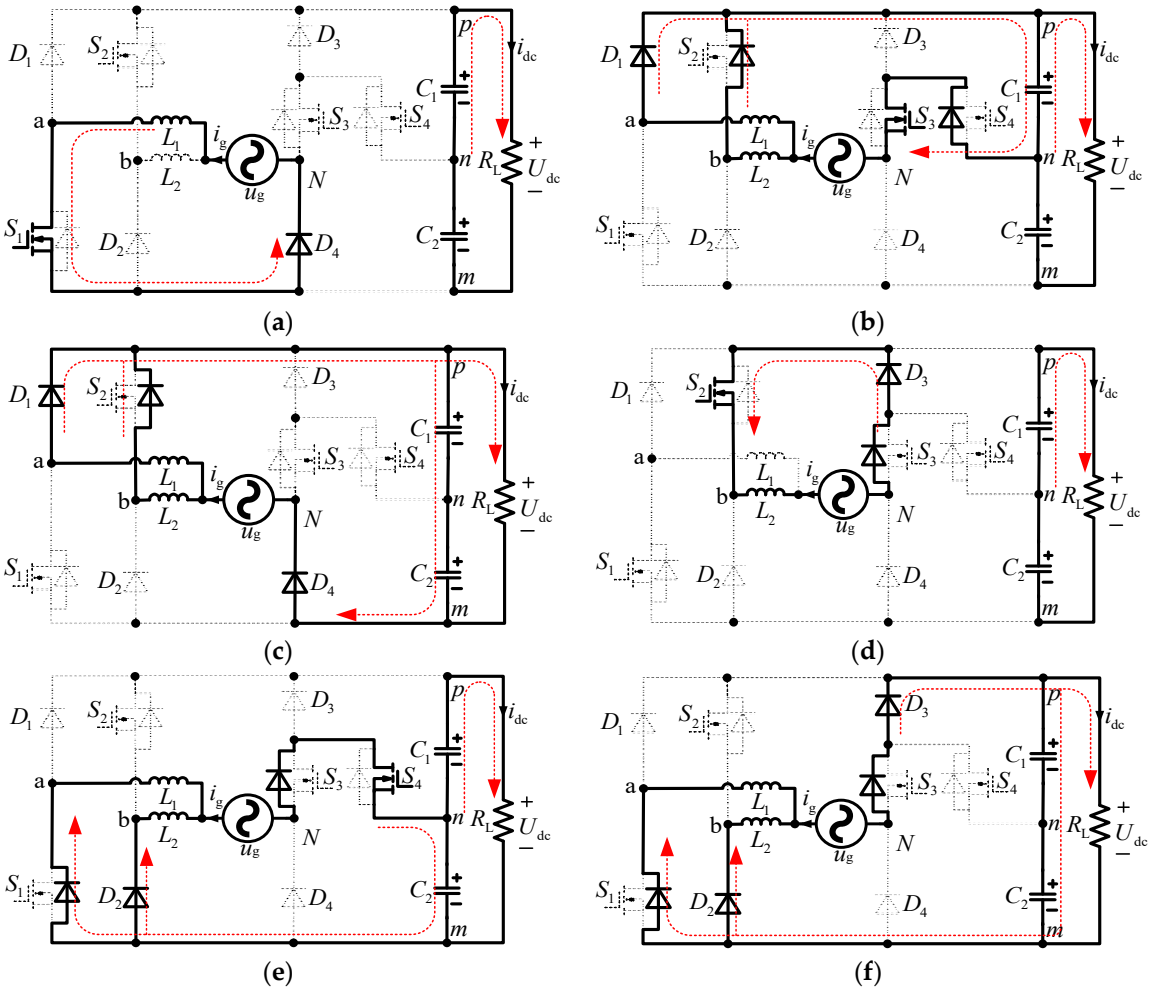

Figure 6. The six working mode of PDBC-II. (**a**) Working mode 1; (**b**) Working mode 2; (**c**) Working mode 3; (**d**) Working mode 4; (**e**) Working mode 5; (**f**) Working mode 6.

Based on the six working mode analysis above, the switching pulse distribution of PDBC-II is summarized, as shown in Table 1. Where "0" and "1" represent switching off and on, "↑" and "↓" represent capacitor charging and discharging, respectively. It can be seen from Table I that the PDBC-II has at most one switch ON in each mode, so the PDBC-II has a lower conduction loss.

Table 1. Switching pulse distribution of PDBC-II.

Mode	i_g	S_1	S_2	S_3	S_4	C_1	C_2	u_{aN}	u_{bN}
1	>0	1	0	0	0	↓	↓	0	u_g
2	>0	0	0	1	0	↑	↓	$U_{dc}/2$	$U_{dc}/2$
3	>0	0	0	0	0	↑	↑	U_{dc}	U_{dc}
4	<0	0	1	0	0	↓	↓	u_g	0
5	<0	0	0	0	1	↓	↑	$-U_{dc}/2$	$-U_{dc}/2$
6	<0	0	0	0	0	↑	↑	$-U_{dc}$	$-U_{dc}$

3. Control and Modulation Strategy

3.1. Control Strategy

In this paper, a double closed loop control system suit for PDBCs is designed, both the voltage outer loop and the current inner loop adopt PI controller. The control block diagram of the PDBCs is

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shown in Figure 7. The transfer function of the PI link in Figure 7 can be expressed as (1), where k_p and k_i are the proportional and integral coefficient, respectively.

$$G_{pi} = (k_p \cdot s + k_i)/s \tag{1}$$

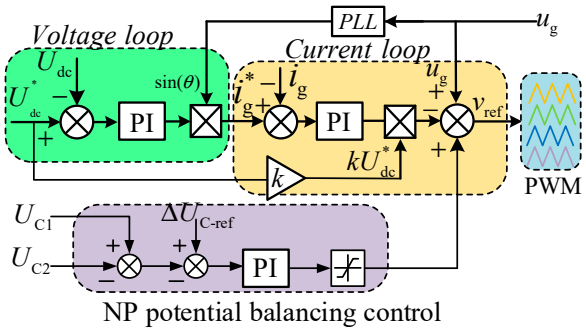

Figure 7. Key waveforms of six working modes in one cycle.

The voltage outer loop is used to keep the output voltage U_{dc} stable, whose output is the reference value of the current inner loop. Firstly, the difference between the DC side voltage U_{dc} and its reference value U_{dc}* is send into the PI controller to obtain an error signal. Then, the error signal is multiply with the phase information of the grid voltage u_g. As a result, the input reference signal i_g* of the current inner loop is obtained.

The current inner loop is used to ensure that the waveform of i_g is sinusoidal and control the power factor close to 1. Firstly, the difference between the AC side current i_g and the reference signal i_g* (the output of the voltage outer loop) is sent to the PI controller. Then, the output of the PI controller is multiply with kU_{dc}*. Finally, its output is taken the difference with the grid voltage ug to get PWM reference signal v_{ref}.

The neutral point (NP) balance of the DC side capacitor is attained by the phase delay control method in this paper. Firstly, the difference between the voltage signals of the capacitors C_1 and C_2 is compared with the reference value. Then, the result is sent to the PI controller to obtain correction signal, which is added to the modulation wave after limiting the amplitude. Therefore, the NP voltage balance is achieved by adjusting the capacitor charging and discharging time.

3.2. Modulation Strategy

In this paper, the multi-carrier PWM modulation strategy is used to generate switching pulse distribution for proposed PDBCs. The PDBC-II is taken as an example to illustrate the switching pulse distribution and bridge arm voltage u_{aN}, u_{bN} of multi-carrier PWM modulation strategy, as shown in Figure 8, where $v_{c1}(t)$, $v_{c2}(t)$, $v_{c3}(t)$, $v_{c4}(t)$, and $v_{ref}(t)$ represent four carrier signals and reference signal, respectively. The reference signal $v_{ref}(t)$ is compared with $v_{c1}(t)$, $v_{c2}(t)$, $v_{c3}(t)$, $v_{c4}(t)$ to obtain the switching pulse waveform of the switches S_1, S_2, S_3, and S_4.

In the positive half-cycle the PWM modulation strategy, the duty cycle can be derived from (2) to (6). Where $U_{g,max}$, T_{on}, and T_{off} is the amplitude of AC voltage, the turn on and off time of the switch, respectively. The modulation ratio M and duty ratio *D* can be defined as follows:

$$M = U_{g,max}/U_{dc} \tag{2}$$

$$D = T_{on}/(T_{on} + T_{off}) \tag{3}$$

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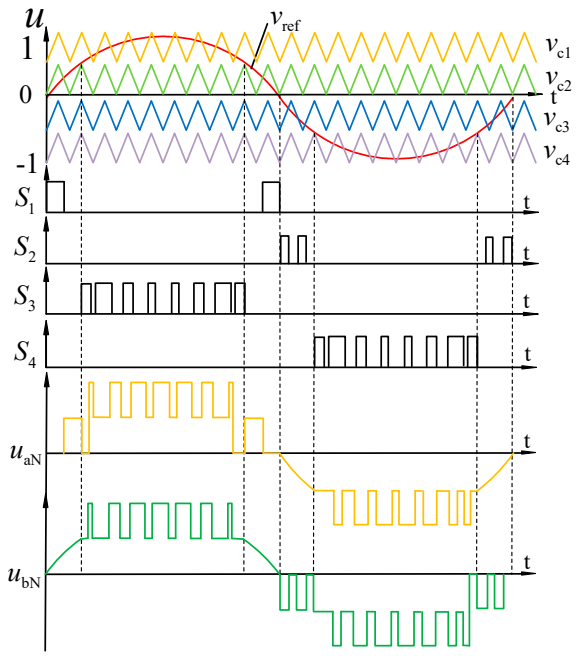

Figure 8. Diagram of modulation strategy.

When $0<v_{ref}(t)<0.5$, the PDBCs operate alternately in working mode 1 and working mode 2. At this time, the inductance volt-second balance has the following relationship:

$$\left(u_g - 0.5U_{dc}\right)\cdot T_{on} = \left(U_{dc} - u_g\right)\cdot T_{off} \tag{4}$$

The duty cycle D_1 is derived from (2) to (4):

$$D_1 = 1 - 2M\sin\left(wt\right) \tag{5}$$

Similarly, when $0.5<v_{ref}(t)<1$, the PDBCs operate alternately in working mode 2 and working mode 3. The duty cycle D_2 can be obtained as follows:

$$D_2 = 2 - 2M\sin\left(wt\right) \tag{6}$$

Based on (5) and (6), when PDBCs operates in the positive half-cycle, the duty cycle change curve is shown in Figure 9. Where the green curve represents the duty cycle D_1, the yellow curve represents the duty cycle D_2, θ_1 and θ_2 are the two angles of alternation between $v_{c1}(t)$ and $v_{c2}(t)$.

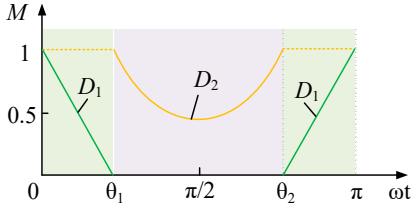

Figure 9. Change curve of duty cycle in the positive half-cycle.

It is assumed that, the amplitude of $v_{ref}(t)$ is 1 (after normalization), the θ_1 and θ_2 can be calculated as follows:

$$\theta_1 = \arcsin 0.5 = \frac{\pi}{6} \tag{7}$$

$$D_2 = 2 - 2M\sin\left(wt\right) \tag{8}$$

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4. Performance Analysis

4.1. Voltage Stress Analysis

Based on the working mode analysis of Figure 6, the switches and diodes voltage stress of three PDBCs are summarized, as shown in Table 2. It can be seen from Table 2 that part of the components voltage stress on the three level bridge is reduced by half. In addition, the PDBC-II and PDBC-III have three components voltage stress reduced by half, while PDBC-I only have two components voltage stress reduced by half. Therefore, in terms of cost, PDBC-II and PDBC-III have the lower cost compared with PDBC-I.

Table 2. Voltage stress of three PDBCs.

Components	PDBC-I	PDBC-II	PDBC-III
$S_{1,2}$	U_{dc}	U_{dc}	U_{dc}
$S_{3,4}$	$U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$
$D_{1,2}$	U_{dc}	U_{dc}	U_{dc}
D_3	U_{dc}	$U_{dc}/2$	U_{dc}
D_4	U_{dc}	U_{dc}	$U_{dc}/2$

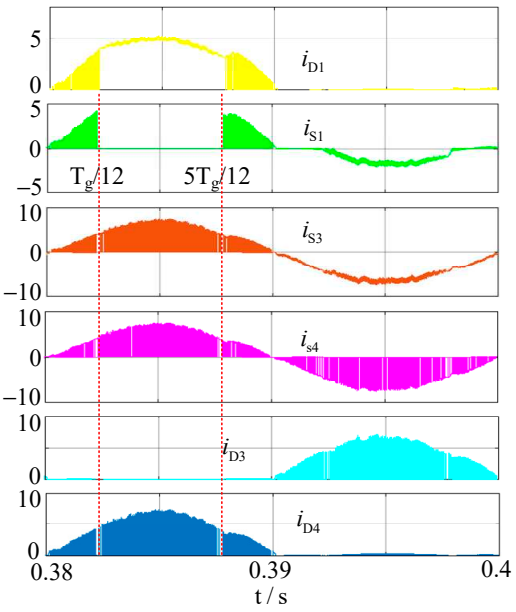

Figure 10. The current stress of PDBC-II.

4.2. Current Stress Analysis

To estimate the conduction loss of the switches and diodes, it is necessary to calculate the average value and the root mean square (RMS) value of the current flowing through the switches and diodes. In this section, PDBC-II is taken as an example to conduct the current stress analysis. Figure 10 shows the current stress simulation waveform of PDBC-II in the Matlab/Simulink environment. It is easy to know from Figure 9, the switching times of two duty cycle D_1, D_2 in Figure 10 are $T_g/12$ and $5T_g/12$ (T_g is one power frequency cycle), respectively. Based on Figure 10, the theoretical derivation of the average value and RMS value of the current flowing through the semiconductor device can be shown as (9) to (18). For the following calculations, it is assumed that the AC side current is a sine wave, the DC side voltage remains unchanged, and the switching frequency f_s is much greater than the grid frequency f_g.

The RMS and average value of diode D_1, D_2 current is calculated by (9):

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$$\begin{cases} I^{2}_{\mathrm{D1,2,rms}} = \dfrac{2}{T_{\mathrm{g}}}\left[\displaystyle\int_{0}^{\frac{T_{\mathrm{g}}}{12}}(1-D_1)\cdot i_{\mathrm{g}}{}^{2}dt + \int_{\frac{T_{\mathrm{g}}}{12}}^{\frac{T_{\mathrm{g}}}{4}}\left(\frac{i_{\mathrm{g}}+0.5I_{\mathrm{g,max}}}{2}\right)^{2}dt\right] \\ I_{\mathrm{D1,2,avg}} = \dfrac{2}{T_{\mathrm{g}}}\left[\displaystyle\int_{0}^{\frac{T_{\mathrm{g}}}{12}}(1-D_1)\cdot i_{\mathrm{g}}dt + \int_{\frac{T_{\mathrm{g}}}{12}}^{\frac{T_{\mathrm{g}}}{4}}\left(\frac{i_{\mathrm{g}}+0.5I_{\mathrm{g,max}}}{2}\right)dt\right] \end{cases} \tag{9}$$

Substituting (5) into (9), the RMS and average values of diodes D_1, D_2 can be obtained:

$$\begin{cases} I_{\mathrm{D1,2,rms}} = \dfrac{\sqrt{6}I_{\mathrm{g,max}}}{24\sqrt{\pi}}\cdot\sqrt{6\pi+15\sqrt{3}+\left(128-72\sqrt{3}\right)M} \\ I_{\mathrm{D1,2,avg}} = \dfrac{I_{\mathrm{g,max}}}{12\pi}\cdot\left[\pi+3\sqrt{3}+\left(2\pi-3\sqrt{3}\right)M\right] \end{cases} \tag{10}$$

The RMS and average value of MOSFET S_1, S_2 current is calculated by (11):

$$\begin{cases} I^{2}_{\mathrm{S1,2,rms}} = \dfrac{2}{T_{\mathrm{g}}}\left[\displaystyle\int_{0}^{\frac{T_{\mathrm{g}}}{12}}D_1\cdot i_{\mathrm{g}}{}^{2}dt + \int_{\frac{7T_{\mathrm{g}}}{12}}^{\frac{3T_{\mathrm{g}}}{4}}\left(\frac{i_{\mathrm{g}}+0.5I_{\mathrm{g,max}}}{2}\right)^{2}dt\right] \\ I_{\mathrm{S1,2,avg}} = \dfrac{2}{T_{\mathrm{g}}}\left[\displaystyle\int_{0}^{\frac{T_{\mathrm{g}}}{12}}D_1\cdot i_{\mathrm{g}}dt + \int_{\frac{7T_{\mathrm{g}}}{12}}^{\frac{3T_{\mathrm{g}}}{4}}\left|\frac{i_{\mathrm{g}}+I_{\mathrm{g,max}}}{2}\right|dt\right] \end{cases} \tag{11}$$

Substituting (5) into (11), the RMS and average values of MOSFET S_1, S_2 can be obtained:

$$\begin{cases} I_{\mathrm{S1,2,rms}} = \dfrac{\sqrt{6}I_{\mathrm{g,max}}}{24\sqrt{\pi}}\cdot\sqrt{14\pi-21\sqrt{3}+\left(72\sqrt{3}-128\right)M} \\ I_{\mathrm{S1,2avg}} = \dfrac{I_{\mathrm{g,max}}}{12\pi}\cdot\left[12-\pi-3\sqrt{3}+\left(3\sqrt{3}-2\pi\right)M\right] \end{cases} \tag{12}$$

The RMS and average value of MOSFET S_3 current is calculated by (13):

$$\begin{cases} I^{2}_{\mathrm{S3,rms}} = \dfrac{4}{T_{\mathrm{g}}}\left[\displaystyle\int_{0}^{\frac{T_{\mathrm{g}}}{12}}D_1\cdot i_{\mathrm{g}}{}^{2}dt + \int_{\frac{T_{\mathrm{g}}}{12}}^{\frac{T_{\mathrm{g}}}{4}}D_2\cdot i_{\mathrm{g}}{}^{2}dt + \int_{\frac{T_{\mathrm{g}}}{2}}^{\frac{3T_{\mathrm{g}}}{4}}i_{\mathrm{g}}{}^{2}dt\right] \\ I_{\mathrm{S3,avg}} = \dfrac{2}{T_{\mathrm{g}}}\left[\displaystyle\int_{0}^{\frac{T_{\mathrm{g}}}{12}}D_1\cdot i_{\mathrm{g}}dt + \int_{\frac{T_{\mathrm{g}}}{12}}^{\frac{T_{\mathrm{g}}}{4}}D_2\cdot i_{\mathrm{g}}dt + \int_{\frac{T_{\mathrm{g}}}{2}}^{\frac{3T_{\mathrm{g}}}{4}}\left|i_{\mathrm{g}}\right|dt\right] \end{cases} \tag{13}$$

Substituting (5) and (6) into (13), the RMS and average values of MOSFET S_3 can be obtained:

$$\begin{cases} I_{\mathrm{S3,rms}} = \dfrac{I_{\mathrm{g,max}}}{2\sqrt{3\pi}}\cdot\sqrt{3\sqrt{3}+10\pi-32M} \\ I_{\mathrm{S3,avg}} = \dfrac{I_{\mathrm{g,max}}}{\pi}\cdot\left(\sqrt{3}+2-\pi M\right) \end{cases} \tag{14}$$

The RMS and average value of MOSFET S_4 current is calculated by (15):

$$\begin{cases} I^{2}_{\mathrm{S4,rms}} = \dfrac{4}{T_{\mathrm{g}}}\left[\displaystyle\int_{0}^{\frac{T_{\mathrm{g}}}{12}}D_1\cdot i_{\mathrm{g}}{}^{2}dt + \int_{\frac{T_{\mathrm{g}}}{12}}^{\frac{T_{\mathrm{g}}}{4}}D_2\cdot i_{\mathrm{g}}{}^{2}dt\right] \\ I_{\mathrm{S4,avg}} = \dfrac{4}{T_{\mathrm{g}}}\left[\displaystyle\int_{0}^{\frac{T_{\mathrm{g}}}{12}}D_1\cdot i_{\mathrm{g}}dt + \int_{\frac{T_{\mathrm{g}}}{12}}^{\frac{T_{\mathrm{g}}}{4}}D_2\cdot i_{\mathrm{g}}dt\right] \end{cases} \tag{15}$$

Substituting (5) and (6) into (15), the RMS and average values of MOSFET S_4 can be obtained:

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$$\begin{cases} I_{\mathrm{S4,rms}} = \dfrac{I_{\mathrm{g,max}}}{2\sqrt{3\pi}} \cdot \sqrt{3\sqrt{3}+10\pi-32M} \\ I_{\mathrm{S4,avg}} = \dfrac{I_{\mathrm{g,max}}}{\pi} \cdot \left(\sqrt{3}+2-\pi M\right) \end{cases} \tag{16}$$

The RMS and average value of diode D_3, D_4 current is calculated by (17):

$$\begin{cases} I^{2}_{\mathrm{D3,4,rms}} = \dfrac{2}{T_{\mathrm{g}}}\left[\int_{0}^{\frac{T_{\mathrm{g}}}{12}}(1-D_1)\cdot i_{\mathrm{g}}{}^{2}dt + \int_{\frac{T_{\mathrm{g}}}{12}}^{\frac{T_{\mathrm{g}}}{4}}(1-D_2)\cdot i_{\mathrm{g}}{}^{2}dt\right] \\ I_{\mathrm{D3,4,avg}} = \dfrac{4}{T_{\mathrm{g}}}\left[\int_{0}^{\frac{T_{\mathrm{g}}}{12}}(1-D_1)\cdot i_{\mathrm{g}}dt + \int_{\frac{T_{\mathrm{g}}}{12}}^{\frac{T_{\mathrm{g}}}{4}}(1-D_2)\cdot i_{\mathrm{g}}dt\right] \end{cases} \tag{17}$$

Substituting (5) and (6) into (17), the RMS and average values of diodes D_3, D_4 can be obtained:

$$\begin{cases} I_{\mathrm{D3,4,rms}} = \dfrac{I_{\mathrm{g,max}}}{2\sqrt{6\pi}} \cdot \sqrt{32M-3\sqrt{3}-4\pi} \\ I_{\mathrm{D3,4,avg}} = \dfrac{I_{\mathrm{g,max}}}{2\pi} \cdot \left(\pi M-\sqrt{3}\right) \end{cases} \tag{18}$$

Figure 11 shows the change curve of the average value and RMS value of the switches and diodes with the modulation ratio M after normalization of $I_{g,max}$. It can be seen from Figure 11 that the current RMS value and average value of each components have the same trend. Since $I_{g,max}$ are normalized, the trend shown in Figure 11 is also applicable under different power levels, which is of great significance for studying the working principle of the rectifier.

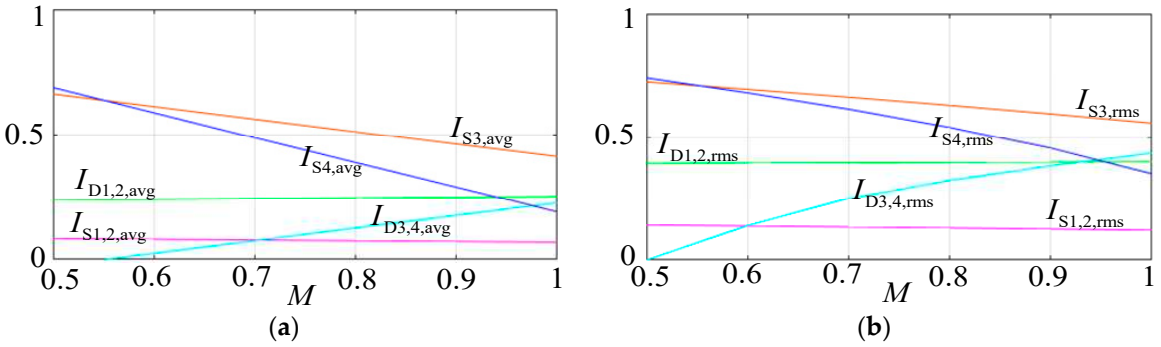

Figure 11. Power component average & RMS current stress as functions of the modulation ratio M normalized: $I_{g,max}$. (**a**) Average value; (**b**) RMS value.

To verify the correctness of the current stress formula deduced in this paper, the current stress value of the switches and diodes is measured in Matlab/Simulink environment under 1kW power rate. Figure 12 shows the comparison between the calculated value and the simulated value of the current stress. It can be seen from Figure 12, the calculated current stress in this paper is consistent with the simulated value, which verifies the correctness of the current stress formula.

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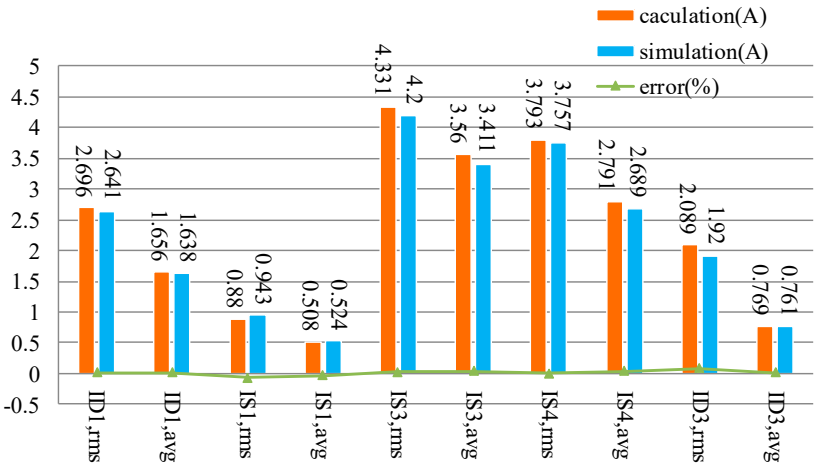

Figure 12. Current stress comparison of calculated and simulated value.

4.3. Loss Analysis

Based on the above current stress analysis, this section analyzes the loss and efficiency of the proposed PDBCs. The losses of MOSFET mainly include conduction losses and switching losses. When the MOSFET is on-state, the on-state resistance r_{ds} resulting the conduction losses. The conduction losses P_{con} can be calculated as (19), where $I_{S,rms}$ is the RMS value of the current flowing through the MOSFET, which can be obtained from the current stress analysis.

$$P_{con} = I_{S,rms}{}^2 \cdot r_{ds} \tag{19}$$

During the drain current and voltage conversion process of the MOSFET, the switching losses is generated. The switching losses which can be calculated by (20), where U_{in}, I_o, t_{on}, t_{off}, and f_s are the RMS value of the input voltage, the output current, the switching process drain current and voltage conversion crossover time, and the switching frequency, respectively.

$$P_{sw} = 0.5U_{in} \cdot I_o \cdot (t_{on} + t_{off}) f_s \tag{20}$$

Similarly, the power losses of the diode in a cycle consists mainly of static losses and dynamic losses. For the static losses, since the fast recovery diode is employed in this paper, there is only the on-state losses are considered. The dynamic losses of the diode can be calculated with (21), where U_f is the forward conduction voltage, $I_{D,avg}$ is the average value of the diode.

$$P_{Son} = \int_0^{T_g} u \cdot i dt \Big/ T_g = U_f \cdot I_{D,avg} \tag{21}$$

Compared with the reverse recovery time t_r, the forward recovery time t_f is negligible, therefore the turn-on losses can be ignored. The turn-off losses can be calculated with (22), where U_{rp} and I_{rp} are the reverse peak voltage and current, t_b is the reverse current fall time.

$$P_{Doff} = \int_{t_0}^{t_2} u_F(t) \cdot i_F(t) dt \Big/ T_S = 0.5U_{rp} I_{rp} t_b f_s \tag{22}$$

In this paper, the MOSFETs and diodes employ IRFP450 and RHRP3060, respectively. According to the data sheet, the parameters for IRFP450 and RHRP3060 are shown in Table 3. The switching frequency f_s=20kHz.

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Table 3. Component parameters.

Components	Parameters	Values
IRFP450	The on-state resistance r_{ds}	0.4Ω
	The on-delay time $t_{d(on)}$	17ns
	The rise time t_r	47ns
	The turn-off delay time $t_{d(off)}$	92ns
	The fall time t_f	44ns
RHRP3060	The conduction voltage U_f	1.7V
	The reverse peak voltage U_{rp}	600V
	The reverse peak current I_{rp}	250μA
	The reverse current fall time t_b	18ns

Based on (9) to (22), the losses of the proposed three PDBCs and CFLC at different output power are calculated respectively. According to the results of the losses calculation, the efficiency diagram at different output power rate is generated, as shown in Figure 13. It can be seen from Figure 13, the four circuits reach peak efficiency around 300W. However, when the output power is over 300W, the efficiency declines slowly as the output power increase. The peak efficiency of PDBC-I is 98.27%, which is the highest in the four circuits. In addition, as the output power level increases, the efficiency of the PDBC-I reaches the highest of the four circuits. Therefore, PDBC-I is more suitable at higher power rate.

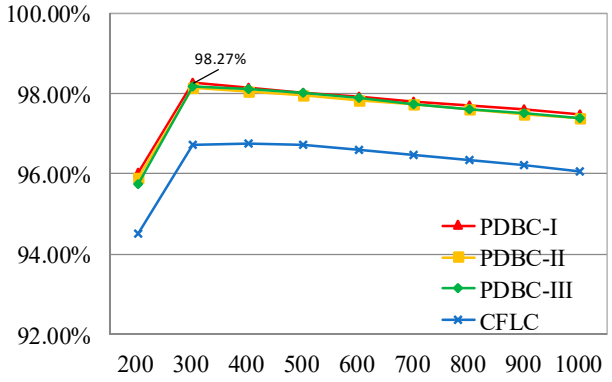

Figure 13. Diagram of efficiency analysis.

5. Experimental Verification

In order to verify the feasibility of the PDBC proposed in this paper and the correctness of the theoretical analysis, PDBC-II [shown in Figure 4(b)] is selected for corresponding experimental verification, as shown in Figure 14. The experimental circuit design mainly includes EMI circuit, auxiliary power supply, main power circuit, signal sampling circuit, MOSFET drive circuit, and protection control circuit. The circuit experimental parameters are shown in Table 4, the controller employ DSP28335, the MOSFETs and diodes employ IRFP450 and RHRP3060, respectively.

Table 4. Main parameters.

Parameters	Label	Value
The input filter inductors	L_1, L_2	2mH
The DC-side capacitors	C_1, C_2	1000μF
The input voltage	u_g	RMS 220V
The output voltage	U_{dc}	400V

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The rated output power	P_o	1000W
The grid frequency	f_g	50Hz
The switching frequency	f_s	20kHz

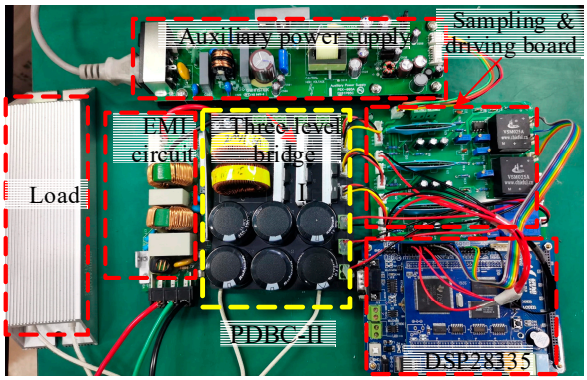
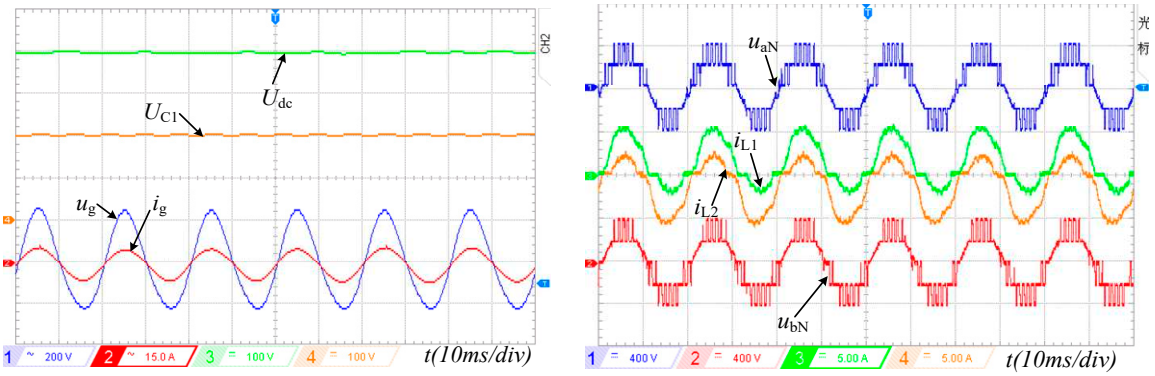


Figure 14. Experimental platforms.

Figure 15 shows the PDBC-II steady-state experimental waveforms of the input and output sides at 1kW rated power. Figure 15a shows the voltage waveforms of the single-phase AC power supply voltage u_g, the input side current i_g, and the DC side voltage U_{dc}, U_{C1}, U_{C2}. As seen from Figure 15a, the input power supply voltage u_g is in phase with the input side current i_g, and it is consistent to achieve power factor correction. The DC side voltage U_{dc} is stable at 400V, and the capacitor voltage U_{C1}, U_{C2} remains dynamically balanced at 200V. Figure 15b shows the bridge arm voltage u_{aN}, u_{bN} waveform and the input inductor current i_{L1}, i_{L2} waveform. As can be seen from Figure 15b, the waveform of inductor current i_{L1} phase ahead 180° of inductor current i_{L2}. Similarly, the bridge arm voltage u_{aN}, u_{bN} waveform changes in positive and negative half-cycles alternately, which is consistent with Figure 6 and Table 1.



(**a**) (**b**)

Figure 15. Steady-state experimental waveforms. (**a**) The voltage waveforms of power supply voltage u_g, current i_g, and the DC side voltage U_{dc}, U_{C1}, U_{C2}; (**b**) The bridge arm voltage u_{aN}, u_{bN} and the inductor current i_{L1}, i_{L2}.

Figure 16 shows the PDBC-II switching pulse distribution experimental waveform. As can be seen from Figure 16, the switches S_1-S_4 has a short high-frequency switching time. As a result, the switching losses of PDBC-II is relatively low. In addition, the switches S_3 and S_4 symmetrically action in positive and negative half-cycle, which is consistent with the switching pulse distribution of Table 1.

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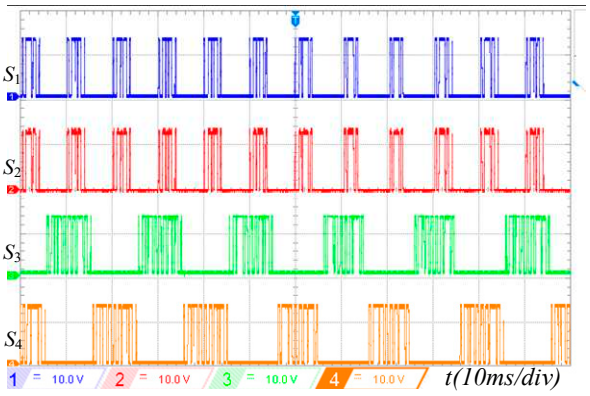
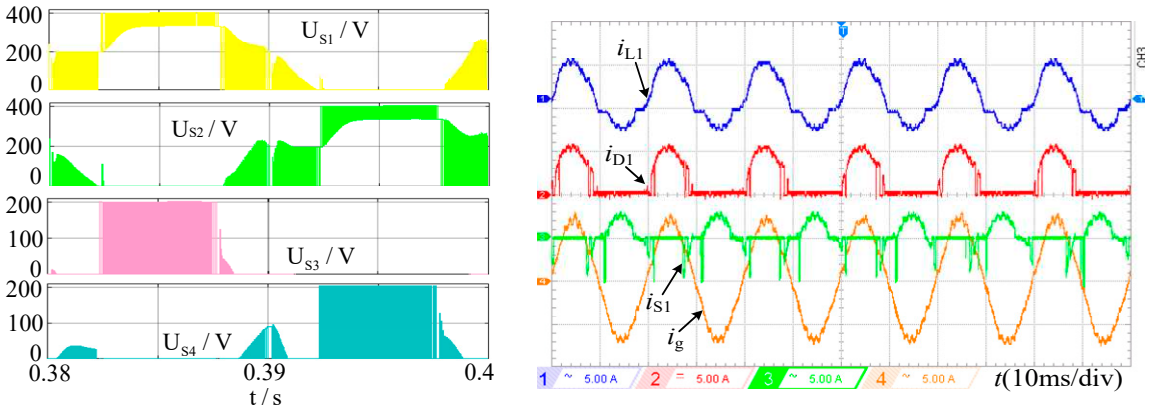


Figure 16. Switching pulse distribution experimental waveform.

Figure 17 shows the PDBC-II voltage and current stress experimental waveforms of the switches at 1kW rated power. Figure 17a shows the voltage stress waveform of the switches S_1-S_4. It can be seen from Figure 17a that the maximum voltage stress of the four switches U_{S1}=U_{S2}≈400V, U_{S3}=U_{S4}≈200V, i.e. the partial voltage stress is halved, which is consistent with the voltage stress analysis in Table 2. Figure 17b shows the waveform of the inductor current, diode D_1 current i_{D1}, the switch S_1 current i_{S1}. As can be seen from Figure 17b, the switch current i_{S1} waveform is enveloped by the inductor L_1 current i_{L1} waveform in the positive half cycle. In addition, the current i_{D1}, i_{S1} changes at high frequencies during the [0, T_g/12] and [5T_g/12, T_g/2] (where T_g is the grid period), which is the same as the simulation waveforms in Figure 10.



(**a**) (**b**)

Figure 17. Voltage and current stress experimental waveforms. (**a**) The voltage stress waveform of switches S_1-S_4; (**b**) The inductor current i_{L1}, diode D_1 current i_{D1}, and the switch S_1 current i_{S1}.

Figure 18 shows the THD test results of PDBC-II at 1kW rated power. As can be seen from Figure 18, at the switching frequency of 20kHz, the THD of PDBC-II is 3.2%, which meets the IEC 6100-3-2 standard.

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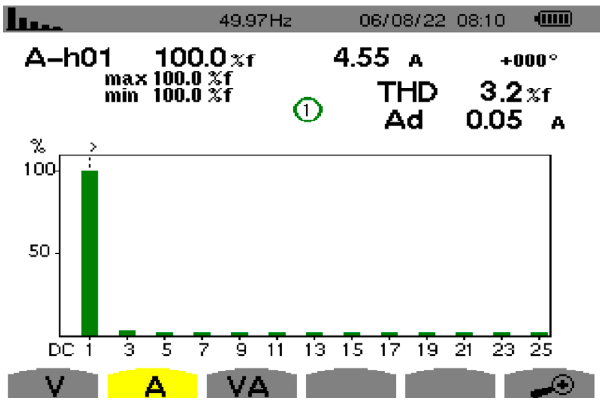

Figure 18. THD test results of PDBC-II.

6. Conclusions

In this paper, combining the three-level PTP circuit and the five-level NPC bridge arm, a family of PDBCs is proposed by transforming the NPC bridge arm. The proposed circuit reduces the volume of the filter inductor to increase the power density of the circuit and improves the working efficiency of the circuit. Through comparative analysis of voltage and current stress, loss, the following conclusions are drawn.

1) The experimental results show that the PDBCs proposed in this paper has a good input and output waveform at low switching frequency. Therefore, the PDBCs can improve overall efficiency by reducing switching losses.

2) The efficiency of the five PDBCs proposed in this paper is higher than CFLC. The PDBC-I has the smallest loss and the highest efficiency, with a peak efficiency of 98.27%, and its overall performance is the best.

3) Compared with the conventional three-level PTP circuit, the five PDBCs proposed in this paper have higher power density, and the voltage stress of some devices is reduced by half. In addition, the PDBC-II and PDBC-III more devices have the voltage stress halved, so their cost is lower.

Conflicts of Interest: The authors declare no conflict of interest.

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