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*Article*

# An Optimal Switching Sequence Model Predictive Control Scheme for the 3L-NPC with Output LC filter

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**Abstract:** In some applications of microgrid and distributed generation, it is required to feed islanded or stand-alone loads with high-quality voltage to provide low total harmonic distortion (THD). To fulfil these demands, an *LC* filter is connected to the output terminals of power electronics converters. A cascaded voltage and current control loop with pulse-width modulation schemes are used to regulate the voltage and current in these systems. However, these strategies have some drawbacks, particularly when multiple-input multiple-output plants (MIMO) are controlled using single-input single-output (SISO) design methods. This methodology usually produces a sluggish transient response and cross-coupling between different control loops. In this paper, a model predictive control (MPC) strategy based on the concept of optimal switching sequences (OSS) is designed to control voltage and current in an LC filter connected to a three-level neutral-point clamped converter. The strategy solves two well-formulated optimisation problems to achieve control of the LC filter variables and the voltages of the DC-link capacitors. Hardware-in-the-Loop (HIL) results are obtained to validate the feasibility of the proposed strategy, using a PLECS-RT HIL platform and a DSP Microlab Box controller. In addition to the good dynamic performance of the proposed OSS-MPC, it is demonstrated by the HIL results that the control algorithm is capable of obtaining low total harmonic distortion (THD) in the output voltage for different conditions.

**Keywords:** model predictive control (MPC); optimal switching sequence (OSS); multilevel inverters; optimal control

## 1. Introduction

When power converters are utilised to supply electrical energy to islanded loads, in microgrids or distributed generation applications, typically an *LC* filter is connected at the converter outputs [1–3]. For instance, converters augmented by *LC* filters are used in applications such as uninterruptible power supplies (UPS) [4], energy storage systems [5], motor drives [6], microgrids [7], etc.

When SISO control tools are utilised, to design the control systems of power converters equipped with *LC* filters, typically two cascaded PI or PR control loops are required: an outer voltage control loop, and an inner current control loop [3,8]. The voltage loop computes the reference for the inner current loop, and the current loop computes the desired converter voltage to be synthesized by a pulse-width modulation (PWM) scheme. However, as discussed in [7], the cascaded interconnection of the voltage and current control loops has some drawbacks. First, because SISO design tools are used, the inner and outer loops are separately designed with different bandwidths to avoid cross-couplings between the dynamics of the voltage and current control loops (usually, the outer loop is one order of

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magnitude slower than the inner loop). This produces a relatively slower transient response. Second, the controllers must be carefully tuned because their parameters affect the system's stability. To overcome the drawbacks of cascaded linear controllers, model predictive control schemes, which are MIMO systems have been recently proposed.

Model Predictive Control (MPC) has been garnering growing interest in the realm of power electronics converter applications. Most common applications include grid-connected converters, inverters with RL load, inverters with output LC filter, and high-performance drives [9]. MPC has several advantages such as simplicity for the inclusion of nonlinearities, simple treatment of constraints, the multivariable case can be easily considered, dead times can be compensated, etc [10]. On the other hand, the disadvantage of MPC is its relatively high computational load, particularly in power converter topologies where a large number of vectors are available. However, the exponential development in the processing power of microprocessors (such as digital signal processors and field-programmable gate arrays) has allowed the implementation of MPC algorithms in real-time platforms [11].

A wide variety of MPC algorithms for power electronics converters exist. An MPC algorithm can be considered, in general terms, as any algorithm that uses a model of the system to predict its future behaviour and select the most appropriate control action based on the solution to an optimal criterion [12]. The optimal criterion is evaluated in a cost function and can be, for example, tracking of the system state variables, minimising common-mode voltage, or reducing the converter switching frequency [12,13]. After the optimal criterion has been reached, and consequently the best possible solution to the optimisation problem has been obtained, the algorithm sends it to the converter to be synthesised.

MPC algorithms are classified according to the nature of the optimisation variable in the control problem. In broad terms, these algorithms for power electronics are classified as Direct MPC or Indirect MPC methods [13]. In direct MPC methods, the optimisation variable is an integer-valued vector representing the state of the converter switching devices. Conversely, in indirect MPC the optimisation variable is a real-valued vector representing the fundamental component of the converter output voltage or duty cycles.

Direct MPC methods are subdivided into three categories: optimal switching vector MPC (OSV-MPC), MPC with hysteresis bounds, and MPC with an implicit modulator. OSV-MPC, commonly named as Finite Control Set MPC (FCS-MPC) in the literature, was firstly proposed to control the output current of a two-level inverter connected to an RL load [14]. Since then, it has been applied to many converter topologies [9]. In this strategy, the converter switches are directly computed and sent to the converter. Thus, allowing direct manipulation of the controlled variables. The advantages of OSV-MPC are an intuitive design procedure, straightforward implementation and fast transient response [13]. However, they come at the cost of high computational complexity, particularly for multilevel power converters, and variable switching frequency due to the absence of a modulator [15].

Direct MPC methods with implicit modulator have been proposed to overcome the issue of variable switching frequency introduced by OSV-MPC while maintaining its advantages [16,17]. These strategies attempt to emulate the behaviour of pulse-width modulation techniques. In particular, Optimal Switching Sequence MPC (OSS-MPC) and Modulated MPC ($M^2PC$) introduce the concept of variable switching time instants [13]. According to the concept of variable switching time instants, the position of the converter switches can change at any moment during a sampling interval. Then, the strategies compute a sequence of switch positions and their corresponding duty cycles to be applied during the next sampling interval. Thus, a fixed switching frequency is achieved resulting in a reduction of harmonic distortion [13]. However, $M^2PC$ is prone to suboptimality because the optimisation problem is solved in two stages: the first stage is to find the optimal switch positions and the second stage is to compute the duty cycles [18].

OSS-MPC avoid suboptimal solutions by computing the optimal sequence of switch positions and their corresponding duty cycles in one stage. The strategy was first introduced for power

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control of a grid-connected two-level inverter [17]. Then, the strategy was modified to be used in other converter topologies such as a three-level neutral-point-clamped (3L-NPC) inverter and vienna rectifier [19–22]. In [23], OSS-MPC was used for voltage control of an LC-filtered two-level inverter achieving low output voltage ripple and reduced harmonic content compared against other MPC methods (such as OSV-MPC). In this paper, the OSS-MPC presented in [22] is extended to three-level neutral-point-clamped (3L-NPC) inverters with output LC filter in standalone operation (such as UPS). The strategy uses a prediction model based on the improved Euler method to compute the future value of the load output voltage and inductor filter current. The predicted values are compared against the desired reference values in the cost function of an optimisation problem. The cost function penalizes the deviation between the measured values and the reference values, and also the control effort of the converter. The optimisation problem is solved offline to compute an optimal switching sequence to be applied by the converter. The optimal switching sequence is then transformed into a three-phase reference signal which is used in an optimisation problem to compute an optimal common-mode voltage to balance the DC-link capacitors of the converter. The common-mode voltage is then added to the three-phase reference signal and the resulting optimal three-phase reference is sent to an In-Phase Disposition PWM scheme to generate the pulses of the switching devices.

## 2. The 3L-NPC Inverter

The 3L-NPC was the first multilevel converter topology, proposed by the group of Akagi in [24]. It was introduced around 1980 to reduce the pulsating torque and harmonic losses on AC drives; thus, improving the efficiency and reducing the cost of the system. Nowadays, this converter topology is the standard for medium and high-voltage applications [25,26]. In the mining industry, for example, 3L-NPC converters are used in variable frequency drives (VFD) for long belt-conveyor systems carrying ore [27].

As shown in the circuit diagram in Figure 1(a), the 3L-NPC converter is composed of four switches and two clamped diodes per leg, producing a total of 27 three-phase switching states $\boldsymbol{u}_{\mathrm{abc}}$ for the whole converter, where $\boldsymbol{u}_{\mathrm{abc}} \in \mathbb{U} \triangleq \{-1, 0, 1\}^3$. As depicted in Figure 1(b), these switching states produce 19 non-redundant and 8 redundant switching vectors (SVs) $\boldsymbol{u}_{\mathrm{s}}$ in the $\alpha\beta$ frame, where $\boldsymbol{u}_{\mathrm{s}} = \mathbf{T}_{\alpha\beta}\boldsymbol{u}_{\mathrm{abc}}$, and $\mathbf{T}_{\alpha\beta}$ is the amplitude invariant *abc*-to-$\alpha\beta$ transformation [28].

According to the circuit diagram depicted in Figure 1(a), the inverter voltages $\boldsymbol{v}_{\mathrm{abc}} = \begin{bmatrix} v_{\mathrm{ao}} & v_{\mathrm{bo}} & v_{\mathrm{co}} \end{bmatrix}^{\intercal}$ are given by

$$\boldsymbol{v}_{\mathrm{abc}} = \frac{1}{2} V_{\mathrm{dc}} \boldsymbol{u}_{\mathrm{abc}} + (1 - |\boldsymbol{u}_{\mathrm{abc}}|) v_{\mathrm{n}} \tag{1}$$

where $|\boldsymbol{u}_{\mathrm{abc}}| = \begin{bmatrix} |u_{\mathrm{a}}| & |u_{\mathrm{b}}| & |u_{\mathrm{c}}| \end{bmatrix}^{\intercal}$, and $v_{\mathrm{n}} = \frac{1}{2}(v_{C2} - v_{C1})$ is the NP-voltage. Using the transformation $\mathbf{T}_{\alpha\beta}$, the inverter voltages (1) in the stationary $\alpha\beta$ frame can be expressed as:

$$\boldsymbol{v}_{\mathrm{s}} = \frac{1}{2} V_{\mathrm{dc}} \boldsymbol{u}_{\mathrm{s}} - \mathbf{T}_{\alpha\beta} |\boldsymbol{u}_{\mathrm{abc}}| v_{\mathrm{n}}. \tag{2}$$

On the other hand, for a three-phase load with a floating neutral, the NP-voltage evolves as a function of the NP-current $i_{\mathrm{n}}$ according to:

$$(C_1 + C_2) \frac{\mathrm{d}v_{\mathrm{n}}}{\mathrm{d}t} = i_{\mathrm{n}}, \quad i_{\mathrm{n}} = |\boldsymbol{u}_{\mathrm{abc}}|^{\intercal} \boldsymbol{i}_{\mathrm{abc}} \tag{3}$$

Therefore, for a given output current $\boldsymbol{i}_{\mathrm{abc}} = \begin{bmatrix} i_s^{\mathrm{a}} & i_s^{\mathrm{b}} & i_s^{\mathrm{c}} \end{bmatrix}^{\intercal}$, as shown in (3), only small- and medium-size SVs, $\boldsymbol{u}_{\mathrm{S}}$ and $\boldsymbol{u}_{\mathrm{M}}$ in Figure 1(b) respectively, can affect the NP-voltage [29]. However, to balance the NP voltage, small SVs play a significant role because the redundancy of each SV drives an NP-current of the same amplitude but in the opposite direction. This tendency impacts $v_{\mathrm{n}}$ but not $\boldsymbol{v}_{\mathrm{s}}$ when the capacitors are balanced with a negligible voltage ripple, i.e., $v_{\mathrm{n}} \approx 0$.

To synthesize a desired inverter output voltage, the three nearest SVs are typically employed in carrier-based and space vector PWM techniques [29,30]. Due to the presence of redundancies, several

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switching sequences (or switching patterns) can synthesize the desired output voltage. Therefore, the generation of switching sequences can be used for several purposes, such as to reduce the switching frequency and to minimize the NP-voltage ripple [29].

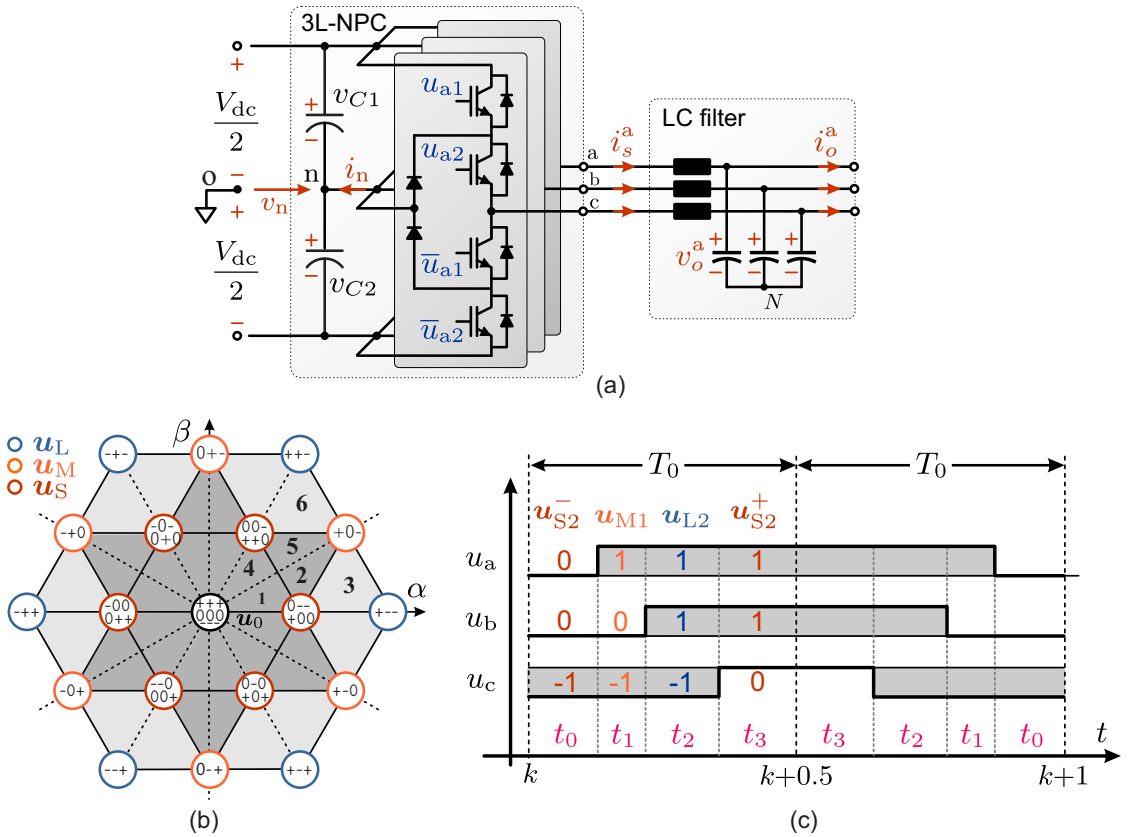


**Figure 1.** 3L-NPC converter: (a) topology; (b) space of switching vectors; (c) 7S-SS for the region $\mathcal{R}_6$.

Based on the above analysis, the seven-segment switching sequence (7S-SS) [29] will be adopted in this work to implement the OSS-MPC strategy for voltage and current control. This switching pattern consists of four SVs, which are arranged in such a way that the transition between two adjacent switching states demands only one switching action. Additionally, each switching period is split into two sub-cycles of duration $T_0{=}T_s/2$, in which the disposition of the second sub-cycle is a reversal of the arrangement of the first [29], as shown in the example in Figure 1(c). Furthermore, the first sub-cycle starts with an N-type small-size SV ($\boldsymbol{u}_S^-$) and ends with the P-type redundancy ($\boldsymbol{u}_S^+$). Therefore, each 7S-SS candidate can be defined accordingly as:

$$\mathcal{S} \triangleq \left\{ \boldsymbol{u}_S^-[t_0], \boldsymbol{u}_1[t_1], \boldsymbol{u}_2[t_2], \boldsymbol{u}_S^+[2t_3], \boldsymbol{u}_2[t_2], \boldsymbol{u}_1[t_1], \boldsymbol{u}_S^-[t_0] \right\} \tag{4}$$

where $t_i$ is the time in which the $i$th switching vector is synthesized by the converter, as depicted in Figure 1(c).

Since the twelve internal regions [highlighted in grey in Figure 1(b)] have two N-type small-size SVs, each of them is further partitioned in two subregions to reduce the NP-voltage ripple [29]. Thus, to determine which dominant N-type small-size SV should be utilised to assemble the desired switching sequence, the space of SVs is divided in 36 regions as shown in Figure 1(b). Then, according to the OSS-MPC principles, a 7S-SS candidate is denoted as $\mathcal{S}_j$, where $j \in \mathcal{R} \triangleq \{1, \ldots, 36\}$.

## 3. Cascaded OSS-MPC Strategy for Voltage and Current Control

In this work, a cascaded OSS-MPC scheme will be employed to simultaneously control the voltage and current at an LC filter, while maintaining balanced voltages at the capacitors of the DC-link in a

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3L-NPC converter. The overall controller is a predictive control scheme based on the solution to two cascaded optimisation problems.

The proposed control scheme is shown in Figure 2. The first optimisation problem —hereinafter called the outer optimisation loop— computes the optimal switching vectors sequence and duty cycles that minimize a cost function. The cost function is designed to track the desired values of the state vector and minimize the control effort of the converter. The second optimisation problem —hereinafter called the inner optimisation loop— computes an optimal common-mode injection signal (see bottom left-hand side of Figure 2). The common-mode injection signal is designed to balance the neutral-point voltage between the DC-link capacitors.

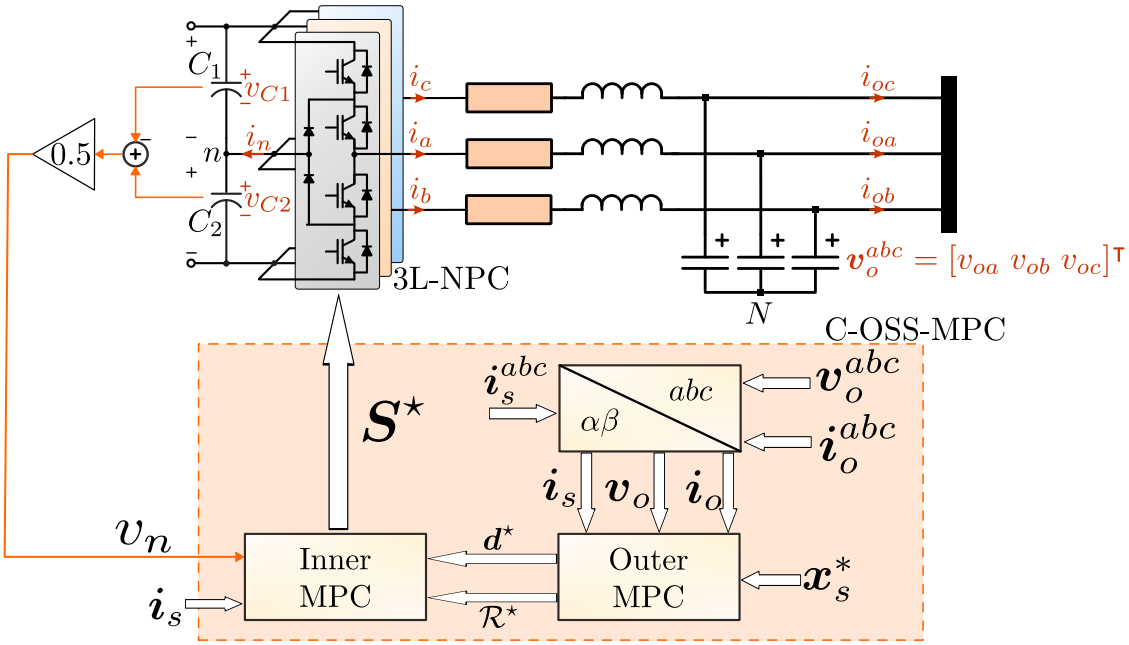


**Figure 2.** Proposed control system, composed of an MPC where the load- voltage and the converter's output current are controlled in a single-stage MPC. Notice that the common mode voltage is obtained using a second MPC algorithm.

### *3.1. Continuous-time model*

Let us consider a three-phase 3L-NPC connected to an LC filter, as shown in Figure 1(a). The system of differential equations describing the dynamics of the LC filter can be written as:

$$L_f \frac{d\boldsymbol{i}_s^{\alpha\beta}}{dt} + R_f \boldsymbol{i}_s^{\alpha\beta} = \boldsymbol{v}_s - \boldsymbol{v}_o^{\alpha\beta} \tag{5a}$$

$$C_f \frac{d\boldsymbol{v}_o^{\alpha\beta}}{dt} = \boldsymbol{i}_s^{\alpha\beta} - \boldsymbol{i}_o^{\alpha\beta} \tag{5b}$$

Assuming that the DC-link NP-voltage is balanced (i.e., $v_n = 0$), the converter output voltage in (2) is equal to $\boldsymbol{v}_s = \frac{V_{dc}}{2}\boldsymbol{u}_s$. Moreover, by rearranging the equations and define the state, input and disturbance vectors as $\boldsymbol{x}_s = [i_s^\alpha\ i_s^\beta\ v_o^\alpha\ v_o^\beta]^\intercal$, $\boldsymbol{u}_s = [u_s^\alpha\ u_s^\beta]^\intercal$, and $\boldsymbol{i}_o = [i_o^\alpha\ i_o^\beta]^\intercal$ (The superscripts $\alpha\beta$ in the vectors will be avoided to simplify the notation). The state-space model of the AC side dynamics is then:

$$\dot{\boldsymbol{x}}_s = \mathbf{A}\boldsymbol{x}_s + \mathbf{B}\boldsymbol{u}_s + \mathbf{E}\boldsymbol{i}_o \tag{6a}$$

$$\boldsymbol{y} = \mathbf{C}\boldsymbol{x}_s \tag{6b}$$

Matrices **A**, **B**, and **E** contain the parameters of the filter and matrix **C** is the identity matrix.

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$$\mathbf{A} = \begin{bmatrix} -\mathbf{L}^{-1}\mathbf{R} & -\mathbf{L}^{-1} \\ \mathbf{C}_f^{-1} & \mathbf{0} \end{bmatrix} \quad \mathbf{B} = \begin{bmatrix} \frac{V_{dc}}{2}\mathbf{L}^{-1} \\ \mathbf{0} \end{bmatrix} \quad \mathbf{E} = \begin{bmatrix} \mathbf{0} \\ -\mathbf{C}_f^{-1} \end{bmatrix} \tag{7}$$

The resistance, inductance, and capacitance matrices are defined as follows:

$$\mathbf{R} = R_f\mathbf{I}_2 \quad \mathbf{L} = L_f\mathbf{I}_2 \quad \mathbf{C}_f = C_f\mathbf{I}_2 \tag{8}$$

The dimensions of the system matrices are $\mathbf{A} \in \mathbb{R}^{4\times4}$, $\mathbf{B} \in \mathbb{R}^{4\times2}$, $\mathbf{E} \in \mathbb{R}^{4\times2}$, $\boldsymbol{x}_s(t) \in \mathbb{R}^{4\times1}$, $\boldsymbol{u}_s(t) \in \mathbb{R}^{2\times1}$, and $\boldsymbol{i}_o(t) \in \mathbb{R}^{2\times1}$.

### *3.2. Discrete-time model*

MPC algorithms use the discrete-time mathematical model of the system, to make predictions of the state vector trajectory, then utilise the predicted values in an optimisation problem and compute the best control action that fulfils the control objectives.

Typically, for the discrete implementation of the continuous-time model, the forward-Euler method is applied. However, as extensively discussed in [31,32], the forward Euler methodology is suitable for implementing nested control loops when two MPC stages are used. For this sort of application an outer MPC algorithm is implemented to regulate the voltages and an inner MPC is utilised to regulate the converter's output currents [31]. Nevertheless, when nested MPC loops are used, two cost functions are required and a global optimum is not necessarily reached (see [32]).

To reach a global optimum, a single cost function for the load voltage and converter's output current is required; therefore, with this approach, a single MPC algorithm is required to regulate the voltage and currents in a single optimisation stage (see Figure 2). However, as extensively discussed in [32], when nested voltage-current control loops are implemented in a single stage, the discrete model implemented using the forward Euler method may produce a lack of causality and controllability in the MPC controller; therefore, other continuous to discrete approximations, for instance, the improved Euler method [33] or a two-steps control horizon [32] are recommended. In this work, the discretization of the continuous-time model is performed using the improved Euler method [33]. This is further discussed in this section.

#### 3.2.1. Forward Euler-Based Discrete Time Model

It is assumed in this work that a 7S-SS is applied to the converter during every switching cycle. Considering the forward Euler method, the instantaneous trajectory of the state vector when a switching vector is applied can be computed as:

$$\boldsymbol{x}_{s(\ell+1)} = \boldsymbol{x}_{s\ell} + T_0 f\left(\boldsymbol{x}_{s\ell}, \boldsymbol{u}_{s\ell}, \boldsymbol{i}_{o\ell}\right) d_\ell \tag{9}$$

where $\ell \in \{0,1,2,3\}$ is the index for the switching vectors of the sequence. The instantaneous evolution of the state vector prediction at the end of the sub-cycle corresponds to its average trajectory when the seven-segment SS defined by (4) (see [20]) is applied to the system:

$$\overline{\boldsymbol{x}}_s[k+1] = \boldsymbol{x}_s[k] + T_0 \sum_{\ell=0}^{3} \left.\frac{d\boldsymbol{x}_s}{dt}\right|_{t=\ell} d_\ell \tag{10}$$

To simplify the analysis, every subinterval slope $m_\ell = f(\boldsymbol{x}_{s\ell}, \boldsymbol{u}_{s\ell}, \boldsymbol{i}_{o\ell})$ is approximated using the values of the state and disturbance vector at the sampling instant $k$ as $m_\ell \approx f(\boldsymbol{x}_s[k], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k])$. Therefore, the prediction of the average trajectory can be expressed as:

$$\overline{\boldsymbol{x}}_s[k+1] = \mathbf{A}_d\boldsymbol{x}_s[k] + \mathbf{E}_d\boldsymbol{i}_o[k] + \mathbf{B}_d \sum_{\ell=0}^{3} \boldsymbol{u}_{s\ell} d_\ell \tag{11}$$

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where $\mathbf{A}_d = \mathbf{I}_4 + T_0\mathbf{A}$, $\mathbf{E}_d = T_0\mathbf{E}$, and $\mathbf{B}_d = T_0\mathbf{B}$. Because for any N-type seven-segment SS, $\boldsymbol{u}_{s0} = \boldsymbol{u}_S^-$, and $\boldsymbol{u}_{s3} = \boldsymbol{u}_S^+$, the duty cycles $d_0$ and $d_3$ can be combined as $d_s = d_0 + d_3$ which is the duty cycle for the small vectors of the sequence [20]. Then, the following linear representation of the average trajectory can be stated as:

$$\overline{\boldsymbol{x}}_s[k+1] = \mathbf{A}_d\boldsymbol{x}_s[k] + \mathbf{E}_d\boldsymbol{i}_o[k] + \mathbf{B}_d\boldsymbol{U}\boldsymbol{d} \tag{12}$$

where the dwell-time vector $\boldsymbol{d}$ and switching matrix $\boldsymbol{U}$ are defined as:

$$\boldsymbol{d} = \begin{bmatrix} d_s & d_1 & d_2 \end{bmatrix} \in \mathbb{D} \triangleq [0,1]^3 \tag{13a}$$

$$\boldsymbol{U} = \begin{bmatrix} \boldsymbol{u}_s & \boldsymbol{u}_1 & \boldsymbol{u}_2 \end{bmatrix} \tag{13b}$$

3.2.2. Improved Euler-Based Discrete Time Model

The improved Euler method is a second-order Runge-Kutta method to compute the solution of ordinary differential equations [33]. In this method, the weighted average of the approximations to the derivative at intermediate points on the solution curve is computed. Specifically, the improved Euler method uses the extreme points of the solution interval (i.e., $k$th and $(k+1)$th points). Higher-order Runge-Kutta methods use more intermediate points to increase the accuracy of the solution.

Once again, it is assumed that a 7S-SS is applied by the converter during the complete switching cycle. Considering the improved Euler method, the instantaneous evolution of the state vector is given by the following equation:

$$\boldsymbol{x}_{s(\ell+1)} = \boldsymbol{x}_{s\ell} + \frac{T_s}{2}\left[f\left(\boldsymbol{x}_{s\ell}, \boldsymbol{u}_{s\ell}, \boldsymbol{i}_{o\ell}\right) + f\left(\boldsymbol{x}_{s\ell}[k+1], \boldsymbol{u}_{s\ell}[k+1], \boldsymbol{i}_{o\ell}[k+1]\right)\right]d_\ell \tag{14}$$

The average slope is multiplied by $T_s$ because it is the time length between predictions in the interval $[k, k+1]$ and predictions in the interval $[k+1, k+2]$. To simplify (14), some assumptions about the states and inputs used for computational purposes are required. Firstly, the slope of the system at the $k$th time instant is computed with the values measured at the time instant $k$ (i.e., $f\left(\boldsymbol{x}_{s\ell}, \boldsymbol{u}_{s\ell}, \boldsymbol{i}_{o\ell}\right) \approx f\left(\boldsymbol{x}_s[k], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k]\right)$). Secondly, the slope at the $(k+1)$th time is computed with the predicted state vector $\overline{\boldsymbol{x}}_s[k+1]$ using the forward Euler approximation defined by (12). The switching sequence applied is the same of time instant $k$ (i.e., $f\left(\boldsymbol{x}_{s\ell}[k+1], \boldsymbol{u}_{s\ell}[k+1], \boldsymbol{i}_{o\ell}[k+1]\right) \approx f\left(\overline{\boldsymbol{x}}_s[k+1], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k+1]\right)$). The disturbance vector is assumed to be constant during the switching cycle, but different between switching cycles (i.e., $\boldsymbol{i}_o[k] \neq \boldsymbol{i}_o[k+1]$). Considering these assumptions, the state vector trajectory is described by:

$$\boldsymbol{x}_{s(\ell+1)} = \boldsymbol{x}_{s\ell} + \frac{T_s}{2}\left[f\left(\boldsymbol{x}_s[k], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k]\right) + f\left(\boldsymbol{x}_s[k+1], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k+1]\right)\right]d_\ell \tag{15}$$

The slopes $\boldsymbol{m}_\ell[k] = f\left(\boldsymbol{x}_s[k], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k]\right)$ and $\boldsymbol{m}_\ell[k+1] = f\left(\overline{\boldsymbol{x}}_s[k+1], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k+1]\right)$ are described by the following equations:

$$\boldsymbol{m}_\ell[k] = \mathbf{A}\boldsymbol{x}_s[k] + \mathbf{B}\boldsymbol{u}_{s\ell} + \mathbf{E}\boldsymbol{i}_o[k] \tag{16a}$$

$$\boldsymbol{m}_\ell[k+1] = \mathbf{A}\overline{\boldsymbol{x}}_s[k+1] + \mathbf{B}\boldsymbol{u}_{s\ell} + \mathbf{E}\boldsymbol{i}_o[k+1] \tag{16b}$$

Replacing $\overline{\boldsymbol{x}}_s[k+1]$ in (16b), the expression for the slope $\boldsymbol{m}_\ell[k+1]$ is obtained as follows:

$$\begin{aligned}\boldsymbol{m}_\ell[k+1] = &\left(\mathbf{A} + \frac{1}{2}T_s\mathbf{A}^2\right)\boldsymbol{x}_s[k] + \frac{1}{2}T_s\mathbf{A}\mathbf{B}\boldsymbol{U}\boldsymbol{d} + \frac{1}{2}T_s\mathbf{A}\mathbf{E}\boldsymbol{i}_o[k] \\ &+ \mathbf{B}\boldsymbol{u}_{s\ell} + \mathbf{E}\boldsymbol{i}_o[k+1]\end{aligned} \tag{17}$$

Then, the average trajectory of the state vector, using the improved Euler method, is computed as:

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$$\overline{\boldsymbol{x}}_s[k+1] = \boldsymbol{x}_s[k] + \frac{T_s}{2}\sum_{\ell=0}^{3}\Big[\boldsymbol{m}_\ell[k] + \boldsymbol{m}_\ell[k+1]\Big]d_\ell \tag{18}$$

Replacing (16a) and (17) into (18), and after some algebraic manipulations, the following expression is obtained:

$$\begin{aligned}\overline{\boldsymbol{x}}_s[k+1] = &\left(\mathbf{I} + T_s\mathbf{A} + \frac{1}{4}T_s^2\mathbf{A}^2\right)\boldsymbol{x}_s + \left(\mathbf{I} + \frac{1}{4}T_s\mathbf{A}\right)T_s\mathbf{B}\boldsymbol{U}\boldsymbol{d} \\ &+ \frac{1}{2}\left(\mathbf{I} + \frac{1}{2}T_s\mathbf{A}\right)T_s\mathbf{E}\boldsymbol{i}_o[k] + \frac{1}{2}T_s\mathbf{E}\boldsymbol{i}_o[k+1]\end{aligned} \tag{19}$$

Equation (19) is useful when an observer-predictor computes $\boldsymbol{i}_o[k+1]$, and the difference between $\boldsymbol{i}_o[k]$ and $\boldsymbol{i}_o[k+1]$ is sufficiently large. However, if it is assumed that $\boldsymbol{i}_o[k] \approx \boldsymbol{i}_o[k+1]$ then the average prediction model is simplified to:

$$\begin{aligned}\overline{\boldsymbol{x}}_s[k+1] = &\left(\mathbf{I} + T_s\mathbf{A} + \frac{1}{4}T_s^2\mathbf{A}^2\right)\boldsymbol{x}_s + \left(\mathbf{I} + \frac{1}{4}T_s\mathbf{A}\right)T_s\mathbf{B}\boldsymbol{U}\boldsymbol{d} \\ &+ \left(\mathbf{I} + \frac{1}{4}T_s\mathbf{A}\right)T_s\mathbf{E}\boldsymbol{i}_o[k]\end{aligned} \tag{20}$$

Discrete-time model in (20) can be written as the linear representation (12) with $\mathbf{A}_d = \mathbf{I} + T_s\mathbf{A} + \frac{1}{4}T_s^2\mathbf{A}^2$, $\mathbf{B}_d = \left(\mathbf{I} + \frac{1}{4}T_s\mathbf{A}\right)T_s\mathbf{B}$, and $\mathbf{E}_d = \left(\mathbf{I} + \frac{1}{4}T_s\mathbf{A}\right)T_s\mathbf{E}$. It is straightforward to show that the discrete-time model obtained in (20) is controllable. Thus, the proposed controller can control the converter currents and the capacitor voltages using a single cost function, avoiding a nested control loop structure.

## 4. C-OSS-MPC formulation

### *4.1. Reference vector*

The objective of the controllers is to keep the voltage of the LC filter capacitors as sinusoidal waveforms. Thus, the reference voltage vector is

$$\boldsymbol{v}_o^*[k+1] = V^* e^{j\omega[k+1]T_s} \tag{21}$$

Where $V^*$ is the magnitude of the reference voltage vector, and $\omega$ is the fundamental frequency of the output voltage ($\omega = 2\pi f_0$). The reference current is obtained as a function of the reference voltage. Replacing the reference voltage vector into the dynamic equation of the output voltages yields:

$$\frac{d\boldsymbol{v}_o^*}{dt} = \frac{1}{C_f}\left(\boldsymbol{i}_s^* - \boldsymbol{i}_o\right) \tag{22}$$

Solving the equation for $\boldsymbol{i}_s^*$ we obtain

$$\boldsymbol{i}_s^* = \omega C_f \mathbf{J}\boldsymbol{v}_o^* + \boldsymbol{i}_o \tag{23}$$

where the matrix $\mathbf{J}$ is defined as

$$\mathbf{J} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \tag{24}$$

It is desirable to constrain the reference current to a maximum value, $I_{max}$. When the amplitude of the reference current is less than the specified limit, the reference current vector is described by equation (23). In the other case, the reference current vector is saturated at $I_{max}$. Therefore, the constrained reference current is represented by the following piece-wise function:

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$$\boldsymbol{i}_s^* = \begin{cases} \omega C_f \mathbf{J} \boldsymbol{v}_o^* + \boldsymbol{i}_o & \|\boldsymbol{i}_s^*\|_2 < I_{max} \\ \frac{I_{max}}{\|\boldsymbol{i}_s^*\|_2} \boldsymbol{i}_s^* & \|\boldsymbol{i}_s^*\|_2 \geq I_{max} \end{cases} \tag{25}$$

Thus, the reference state vector is

$$\boldsymbol{x}_s^*[k+1] = \begin{bmatrix} \boldsymbol{i}_s^* \\ \boldsymbol{v}_o^* \end{bmatrix} \tag{26}$$

*4.2. Cost function*

At the heart of the MPC strategy lies the cost function. In the cost function, the variables related to the control objectives are weighted to choose the best possible action. In FCS-MPC schemes, the cost function is most commonly designed to minimize the tracking error [34]; however, it has been shown that FCS-MPC strategies without penalization of the control effort are equivalent to quantised dead-beat controllers [15]. Deadbeat controller features fast dynamic response [35] but they have poor robustness against model mismatches, parameter uncertainties, and noise on measured variables [36]. To alleviate the unwanted effects of deadbeat controllers, the control effort is usually penalised in the cost function [35]. In the control proposed in this work, the outer MPC loop has two objectives: minimise the tracking error between the state vector and its reference, and penalize the control effort. Therefore, the following cost function is defined:

$$J(\boldsymbol{U}_j, \boldsymbol{d}_j) = \|\boldsymbol{x}_s[k+1] - \boldsymbol{x}_s^*[k+1]\|_{\mathbf{Q}}^2 + \lambda_u \|\boldsymbol{u}[k+1] - \boldsymbol{u}_{ss}\|_2^2 \tag{27}$$

The positive-definite matrix $\mathbf{Q}$ = diag($\lambda_i$,$\lambda_i$,$\lambda_v$,$\lambda_v$) is used to trade-off the control objectives of the state vector tracking. Similarly, the weighting factor $\lambda_u$ is used to penalize the control effort. The optimisation variable of the problem is the average switching vector, $\boldsymbol{u}(k)$. The average switching vector is the product between the switching matrix and duty cycle vector as $\boldsymbol{u}(k) = \boldsymbol{U}\boldsymbol{d}$.

Firstly, the term of the cost function used to penalize the reference tracking error will be reformulated as a function of the average switching vector $\boldsymbol{u}(k)$. Replacing (12) in (27), yields:

$$\|\mathbf{B}_d \boldsymbol{u} - \underbrace{(\boldsymbol{x}_s^*[k+1] - \mathbf{A}_d \boldsymbol{x}_s[k] - \mathbf{E}_d \boldsymbol{i}_o[k])}_{\boldsymbol{\kappa}[k]}\|_{\mathbf{Q}}^2 \tag{28}$$

The second term of the cost function in eq. (27) has the vector $\boldsymbol{u}_{ss}$. Vector $\boldsymbol{u}_{ss}$ is the steady-state control action. The steady-state control action is the input vector needed to drive the system towards the steady-state solution. The expression for this vector is obtained by solving the circuit of Figure 3 for $\boldsymbol{u}_{ss}$. The steady-state control input $\boldsymbol{u}_{ss}$ is defined as:

$$\boldsymbol{u}_{ss} = \frac{2}{V_{dc}} \left\{ \left[ \left(1 - \omega^2 L_f C_f\right) \mathbf{I}_2 + \left(\omega R_f C_f\right) \mathbf{J} \right] \boldsymbol{v}_o^* + \left[ R_f \mathbf{I}_2 + \omega L_f \mathbf{J} \right] \boldsymbol{i}_o \right\} \tag{29}$$

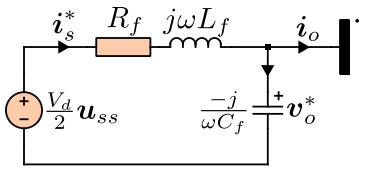


**Figure 3.** Circuit diagram to obtain the steady-state control action.

Finally, the cost function for the optimisation problem can be written as:

$$J_j(\boldsymbol{U}_j, \boldsymbol{d}_j) = \|\mathbf{B}_d \boldsymbol{u}(k) - \boldsymbol{\kappa}\|_{\mathbf{Q}}^2 + \lambda_u \|\boldsymbol{u}(k) - \boldsymbol{u}_{ss}\|_2^2 \tag{30}$$

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### 4.3. Optimisation problem

In OSS-MPC, the optimal switching sequence (OSS) is obtained by solving an optimisation problem. The solution must comply with constraints such that the sum of leg duty cycles is equal to one, and each duty cycle must be equal to or greater than zero. Therefore, the optimisation problem to be solved is the following:

$$\{\boldsymbol{U}^\star, \boldsymbol{d}^\star\} = \arg\min_{\boldsymbol{U}_j} \left\{ \min_{\boldsymbol{d}_j} J_j(\boldsymbol{U}_j, \boldsymbol{d}_j) \right\} \tag{31a}$$

$$\text{s.t.} \quad 1^\intercal \boldsymbol{d} = 1 \tag{31b}$$

$$\boldsymbol{d}_j \geq \mathbf{0} \tag{31c}$$

The optimisation problem has the same form as the one solved in [22]. Therefore, the same optimiser will be used. Thus, the usual strategy to solve MPC problems with 3L-NPC converters of evaluating each region $\mathcal{R}_j \in \{\mathcal{R}_1, \ldots, \mathcal{R}_{24}\}$ of the space of vectors is avoided.

## 5. Solution to the outer optimisation problem

In this section, the relaxed optimisation problem will be solved to obtain the optimal switching vector sequence and its corresponding duty cycles to be applied during the next sampling instant. Two cases of the problem are distinguished; First, the linear modulation stage where the duty cycles are positive. Second, the overmodulation stage where the duty cycle of the small switching vectors becomes negative.

### 5.1. Non-negative duty cycles: the linear modulation stage

#### 5.1.1. Relaxed optimisation problem

To relax the optimisation problem, the inequality constraints are removed from the problem formulation. The relaxed optimisation problem is then stated as

$$\min_{\boldsymbol{d}} \; J_j(\boldsymbol{U}_j, \boldsymbol{d}_j) \tag{32a}$$

$$\text{s.t.} \quad 1^\intercal d = 1 \tag{32b}$$

Expanding the cost function yields:

$$J_j = (\mathbf{B}_d \boldsymbol{u} - \boldsymbol{\kappa})^\intercal \, \boldsymbol{Q} \, (\mathbf{B}_d \boldsymbol{u} - \boldsymbol{\kappa}) + \lambda_u \, (\boldsymbol{u} - \boldsymbol{u}_{ss})^\intercal \, (\boldsymbol{u} - \boldsymbol{u}_{ss}) \tag{33}$$

The following expression is obtained,

$$J_j = \boldsymbol{u}^\intercal \, (\boldsymbol{Q\prime} + \lambda_u \mathbf{I}_2) \, \boldsymbol{u} - 2\boldsymbol{u}^\intercal \, \left( \mathbf{B}_d^\intercal \boldsymbol{Q} \boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss} \right) + \left( \lambda_u \boldsymbol{u}_{ss}^\intercal \boldsymbol{u}_{ss} + \boldsymbol{\kappa}^\intercal \boldsymbol{Q} \boldsymbol{\kappa} \right) \tag{34}$$

where $Q\prime$ is the modified weight matrix, $\mathbf{Q\prime} = \mathbf{B}_d^\intercal \mathbf{Q} \mathbf{B}_d$. The elements of the switching matrix $\boldsymbol{U}_j \in \mathbb{R}^{2\times 3}$ are the vectors of the switching sequence:

$$\boldsymbol{U}_j = \begin{bmatrix} u_{s\alpha} & u_{1\alpha} & u_{2\alpha} \\ u_{s\beta} & u_{1\beta} & u_{2\beta} \end{bmatrix} \tag{35}$$

#### 5.1.2. Solution of the relaxed optimisation problem

Considering the equality constraint of the relaxed optimisation problem, the duty cycles for the small switching vectors, as a function of the remaining duty cycles, can be written as:

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$$d_{Sj} = 1 - d_{1j} - d_{2j} \tag{36}$$

An auxiliar variable, $\boldsymbol{d}_{\eta j}$, is defined to eliminate the dependent variable $d_S$ from the optimisation vector $\boldsymbol{d}_j$:

$$\boldsymbol{d}_{\eta j} = \begin{bmatrix} d_{1j} & d_{2j} \end{bmatrix}^\intercal \tag{37}$$

The relationship between $\boldsymbol{d}_j$ and $\boldsymbol{d}_{\eta j}$ is the following:

$$\boldsymbol{d}_j = \underbrace{\begin{bmatrix} -1 & -1 \\ 1 & 0 \\ 0 & 1 \end{bmatrix}}_{\boldsymbol{M}} \boldsymbol{d}_{\eta j} + \underbrace{\begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}}_{\boldsymbol{N}} \tag{38}$$

Then, $\boldsymbol{u} = \boldsymbol{U}\boldsymbol{d} = \boldsymbol{U}\left(\boldsymbol{M}\boldsymbol{d}_{\eta j} + \boldsymbol{N}\right) = \boldsymbol{U}\boldsymbol{M}\boldsymbol{d}_{\eta j} + \boldsymbol{U}\boldsymbol{N}$ and $\boldsymbol{u}^\intercal = \boldsymbol{d}^\intercal\boldsymbol{U}^\intercal = \left(\boldsymbol{M}\boldsymbol{d}_{\eta j} + \boldsymbol{N}\right)^\intercal\boldsymbol{U}^\intercal = \left(\boldsymbol{d}_{\eta j}^\intercal\boldsymbol{M}^\intercal + \boldsymbol{N}^\intercal\right)\boldsymbol{U}^\intercal$. The cost function in terms of $\boldsymbol{d}_{\eta j}$ is

$$\begin{aligned} J = {} & \boldsymbol{d}_{\eta j}^\intercal\boldsymbol{M}^\intercal\boldsymbol{U}^\intercal\left(\boldsymbol{Q}\prime + \lambda_u\boldsymbol{I}_2\right)\boldsymbol{U}\boldsymbol{M}\boldsymbol{d}_{\eta j} \\ & + 2\boldsymbol{d}_{\eta j}\boldsymbol{M}^\intercal\boldsymbol{U}^\intercal\left(\boldsymbol{Q}\prime + \lambda_u\boldsymbol{I}_2\right)\boldsymbol{U}\boldsymbol{N} \\ & - 2\boldsymbol{d}_{\eta j}\boldsymbol{M}^\intercal\boldsymbol{U}^\intercal\left(\mathbf{B}_d^\intercal\boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u\boldsymbol{u}_{ss}\right) + \boldsymbol{N}^\intercal\boldsymbol{U}^\intercal\left(\boldsymbol{Q}\prime + \lambda_u\boldsymbol{I}_2\right)\boldsymbol{U}\boldsymbol{N} \\ & - 2\boldsymbol{N}^\intercal\boldsymbol{U}^\intercal\left(\mathbf{B}_d^\intercal\boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u\boldsymbol{u}_{ss}\right) + \left(\boldsymbol{\kappa}^\intercal\boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u\boldsymbol{u}_{ss}^\intercal\boldsymbol{u}_{ss}\right) \end{aligned} \tag{39}$$

Computing the gradient of $J$ with respect to $\boldsymbol{d}_{\eta j}$ and making it equal to zero, yields:

$$\begin{aligned} \nabla J\left(\boldsymbol{d}_{\eta j}\right) = {} & 2\boldsymbol{M}^\intercal\boldsymbol{U}^\intercal\left(\boldsymbol{Q}\prime + \lambda_u\boldsymbol{I}_2\right)\boldsymbol{U}\boldsymbol{M}\boldsymbol{d}_{\eta j} \\ & + 2\boldsymbol{M}^\intercal\boldsymbol{U}^\intercal\left(\boldsymbol{Q}\prime + \lambda_u\boldsymbol{I}_2\right)\boldsymbol{U}\boldsymbol{N} \\ & - 2\boldsymbol{M}^\intercal\boldsymbol{U}^\intercal\left(\mathbf{B}_d^\intercal\boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u\boldsymbol{u}_{ss}\right) = \mathbf{0} \end{aligned} \tag{40}$$

Reorganizing (40) to leave the terms related to the duty cycles on the left, (41) is obtained:

$$\begin{aligned} & \boldsymbol{M}^\intercal\boldsymbol{U}^\intercal\left(\boldsymbol{Q}\prime + \lambda_u\boldsymbol{I}_2\right)\boldsymbol{U}\boldsymbol{M}\boldsymbol{d}_{\eta j} = \\ & \boldsymbol{M}^\intercal\boldsymbol{U}^\intercal\left(\mathbf{B}_d^\intercal\boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u\boldsymbol{u}_{ss}\right) - \boldsymbol{M}^\intercal\boldsymbol{U}^\intercal\left(\boldsymbol{Q}\prime + \lambda_u\boldsymbol{I}_2\right)\boldsymbol{U}\boldsymbol{N} \end{aligned} \tag{41}$$

Solving the equation for $\boldsymbol{d}_{\eta j}$ yields:

$$\boldsymbol{d}_{\eta j} = \left[\boldsymbol{U}\boldsymbol{M}\right]^{-1}\boldsymbol{u}_{unc} - \left[\boldsymbol{U}\boldsymbol{M}\right]^{-1}\boldsymbol{U}\boldsymbol{N} \tag{42}$$

The unconstrained control action ($\boldsymbol{u}_{uc}$) is defined as:

$$\boldsymbol{u}_{uc} = \left(\boldsymbol{Q}\prime + \lambda_u\boldsymbol{I}_2\right)^{-1}\left(\boldsymbol{B}_d^\intercal\boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u\boldsymbol{u}_{ss}\right) \tag{43}$$

Now, it is required to map the solution back to its original variables. Replacing (42) in (38), yields:

$$\boldsymbol{d}_{rj} = \begin{bmatrix} \boldsymbol{M}\left(\boldsymbol{U}\boldsymbol{M}\right)^{-1} & \boldsymbol{N} - \boldsymbol{M}\left(\boldsymbol{U}\boldsymbol{M}\right)^{-1}\boldsymbol{U}\boldsymbol{N} \end{bmatrix}\begin{bmatrix} \boldsymbol{u}_{uc} \\ 1 \end{bmatrix} \tag{44}$$

The optimal duty cycles for the linear modulation stage are computed using the $(3 \times 3)$ matrix:

$$\boldsymbol{d}_{rj} = \frac{1}{\Delta}\begin{bmatrix} u_{1\beta} - u_{2\beta} & u_{2\alpha} - u_{1\alpha} & \boldsymbol{u}_1 \times \boldsymbol{u}_2 \\ u_{2\beta} - u_{s\beta} & u_{s\alpha} - u_{2\alpha} & \boldsymbol{u}_2 \times \boldsymbol{u}_s \\ u_{s\beta} - u_{1\beta} & u_{1\alpha} - u_{s\alpha} & \boldsymbol{u}_s \times \boldsymbol{u}_1 \end{bmatrix}\begin{bmatrix} u_{uc,\alpha} \\ u_{uc,\beta} \\ 1 \end{bmatrix} \tag{45}$$

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where $\Delta$ is the determinant of matrix product $(\boldsymbol{UM})^{-1}$:

$$\Delta = \boldsymbol{u}_S \times \boldsymbol{u}_1 + \boldsymbol{u}_2 \times \boldsymbol{u}_S + \boldsymbol{u}_1 \times \boldsymbol{u}_2 \tag{46}$$

Where $\boldsymbol{u}_x \times \boldsymbol{u}_y = u_{x\alpha}u_{y\beta} - u_{x\beta}u_{y\alpha}$ denotes the cross product.

## 6. Optimal Solution

In the previous section, the relaxed solution to the optimisation problem was calculated. The relaxed duty cycles vector $\boldsymbol{d}_{rj}$ is the local solution for each region $\mathcal{R}_j \in \mathcal{R}$ of the control hexagon $\mathbb{V}$. The relaxed solution computed with (32) fulfills the equality constraint $1^\intercal \boldsymbol{d} = 1$. Thus, all regions can be mapped onto $\boldsymbol{u}_{uc}$ in the $\alpha\beta$-plane. However, only one region fulfils the non-negativity constraint [20]. The non-negativity constraint can then be considered in the solution with a simple methodology (as reported in [20,22]). The methodology introduced therein also reduces the computational burden avoiding the search over all 24 regions of the control region $\mathbb{V}$ to only four. The methodology will be explained in this section.

Firstly, considering the $\alpha\beta$-plane shown in Figure 4(a) with the Space of Vectors of the 3L-NPC is divided into 12 regions. The algorithm seeks the region where $\boldsymbol{u}_{uc}$ is located, and then the three sectors in that region are evaluated in the control algorithm. Given that $\boldsymbol{u}_{uc}$ is the desired solution of the optimisation problem, its angle is used to find the optimal region in the plane. The optimal sector $\mathcal{S}^\star$ is obtained from the following equation:

$$S^\star = \text{floor}\left\{ \frac{6}{\pi} \tan^{-1}\left( \frac{u_{uc,\beta}}{u_{uc,\alpha}} \right) \right\} + 1 \tag{47}$$

When the optimal sector is calculated, the duty cycles of the switching sequences contained in it are evaluated. The sector whose duty cycles comply with the non-negativity constraint is the optimal sector, and thus, the optimal switching sequence is found.

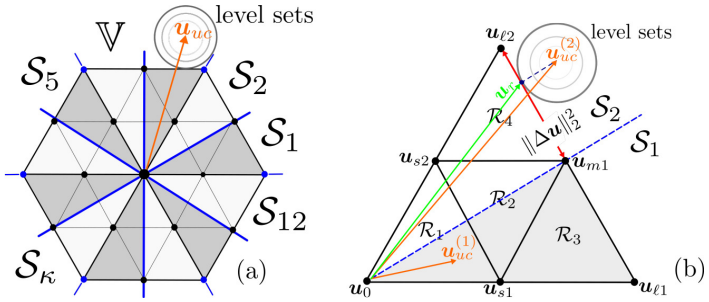


**Figure 4.** Control region of the 3L-NPC. (a) Hexagon divided into 12 sectors to reduce the computational burden of the OSS-MPC algorithm, and (b) close-up look into sectors $\mathcal{S}_1$-$\mathcal{S}_2$.

The conventional enumeration algorithm can be reduced to only 3 regions after the sector has been identified. Each sector has three candidate switching sequences, but only one of them fulfills the non-negativity constraint. Thus, the optimal pair $\{\boldsymbol{U}^\star, \boldsymbol{d}^\star\}$ is found evaluating the non-negativity condition over the duty cycles vector of each candidate region. However, if $\boldsymbol{u}_{uc}$ falls outside the control region $\mathbb{V}$ (e.g., see $\boldsymbol{u}_{uc}^{(2)}$ in Figure 4(b)) then none of the candidate switching sequences fulfil the non-negativity constraint.

The aforementioned case occurs during a transient operation. The candidate switching sequence is then reduced to one and is built by the medium and large switching vectors belonging to the only outer region that intersects the optimal sector. The case is further analyzed in the next subsection.

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### *6.1. Handling the negative duty cycles: the overmodulation stage*

#### 6.1.1. Relaxed optimisation problem

The unconstrained average switching vector goes outside the hexagon, thus the duty cycle for the small switching vector becomes negative. Defining $d_{Sj} = 0$, the optimisation variable becomes

$$\boldsymbol{d}_j = \begin{bmatrix} 0 \\ d_{1j} \\ d_{2j} \end{bmatrix} \tag{48}$$

Consider the equality constraint

$$1^\intercal \begin{bmatrix} 0 & d_{1j} & d_{2j} \end{bmatrix} = 1 \tag{49}$$

Notice that one of the two optimisation variables is dependent. Thus, if we set $d_{2j}$ to be dependent of $d_{1j}$, we can find an auxiliary vector to reduce the equality-constrained optimisation problem into an unconstrained optimisation problem

$$\boldsymbol{d}_j = \underbrace{\begin{bmatrix} 0 \\ 1 \\ -1 \end{bmatrix}}_{\boldsymbol{M\prime}} d_{1j} + \underbrace{\begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix}}_{\boldsymbol{N\prime}} \tag{50}$$

Then, $\boldsymbol{u} = \boldsymbol{U}\boldsymbol{d} = \left(\boldsymbol{M\prime}\boldsymbol{d}_j + \boldsymbol{N\prime}\right) = \left(\boldsymbol{u}_1 - \boldsymbol{u}_2\right) d_1 + \boldsymbol{u}_2$ and $\boldsymbol{u}^\intercal = \boldsymbol{d}_j^\intercal \boldsymbol{U}^\intercal = \left(\boldsymbol{M\prime}\boldsymbol{d}_j + \boldsymbol{N\prime}\right)^\intercal \boldsymbol{U}^\intercal = \left(\boldsymbol{u}_1 - \boldsymbol{u}_2\right)^\intercal d_1 + \boldsymbol{u}_2^\intercal$. The cost function is

$$\begin{aligned} J = & \left(\boldsymbol{u}_1 - \boldsymbol{u}_2\right)^\intercal \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right) \left(\boldsymbol{u}_1 - \boldsymbol{u}_2\right) d_1^2 \\ & + 2 \left(\boldsymbol{u}_1 - \boldsymbol{u}_2\right)^\intercal \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right) \boldsymbol{u}_2 d_1 \\ & - 2 \left(\boldsymbol{u}_1 - \boldsymbol{u}_2\right)^\intercal \left(\mathbf{B}_d^\intercal \boldsymbol{Q} \boldsymbol{u}_{db}^{\prime} + \lambda_u \boldsymbol{u}_{ss}\right) d_1 \\ & + \boldsymbol{u}_2^\intercal \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right) \boldsymbol{u}_2 - 2 \boldsymbol{u}_2^\intercal \left(\mathbf{B}_d^\intercal \boldsymbol{Q} \boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss}\right) \\ & + \left(\boldsymbol{\kappa}^\intercal \boldsymbol{Q} \boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss}^\intercal \boldsymbol{u}_{ss}\right) \end{aligned} \tag{51}$$

#### 6.1.2. Solution of the relaxed optimisation problem

The unconstrained optimisation problem is solved by setting to zero the derivative of the cost function with respect to the optimisation variable

$$\begin{aligned} \frac{d}{d(d_{1j})} J = & 2 \left(\boldsymbol{u}_1 - \boldsymbol{u}_2\right)^\intercal \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right) \left(\boldsymbol{u}_1 - \boldsymbol{u}_2\right) d_1 \\ & + 2 \left(\boldsymbol{u}_1 - \boldsymbol{u}_2\right)^\intercal \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right) \boldsymbol{u}_2 \\ & - 2 \left(\boldsymbol{u}_1 - \boldsymbol{u}_2\right)^\intercal \left(\mathbf{B}_d^\intercal \boldsymbol{Q} \boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss}\right) = 0 \end{aligned} \tag{52}$$

Solving it for $d_1$ yields:

$$d_1 = \frac{\left(\boldsymbol{u}_1 - \boldsymbol{u}_2\right)^\intercal \left(\mathbf{B}_d^\intercal \boldsymbol{Q} \boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss}\right)}{\left(\boldsymbol{u}_1 - \boldsymbol{u}_2\right)^\intercal \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right) \left(\boldsymbol{u}_1 - \boldsymbol{u}_2\right)} - \frac{\left(\boldsymbol{u}_1 - \boldsymbol{u}_2\right)^\intercal \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right) \boldsymbol{u}_2}{\left(\boldsymbol{u}_1 - \boldsymbol{u}_2\right)^\intercal \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right) \left(\boldsymbol{u}_1 - \boldsymbol{u}_2\right)} \tag{53}$$

The matrix $\left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right)$ corresponds to a scalar multiplied by the identity matrix. Bearing on mind that $\boldsymbol{u}_{uc} = \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right)^{-1} \left(\mathbf{B}_d^\intercal \boldsymbol{Q} \boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss}\right)$, the optimal duty cycle $d_1^\star$ is

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$$d_{1j}^{\star} = \frac{(\boldsymbol{u}_1 - \boldsymbol{u}_2)^{\intercal}(\boldsymbol{u}_{uc} - \boldsymbol{u}_2)}{(\boldsymbol{u}_1 - \boldsymbol{u}_2)^{\intercal}(\boldsymbol{u}_1 - \boldsymbol{u}_2)} \tag{54}$$

Notice that the denominator of $d_{1j}^{\star}$ is the length between a large and medium vector in the hexagon frontier (see Figure 4(b)), thus:

$$\|\Delta \boldsymbol{u}\|_2^2 = (\boldsymbol{u}_1 - \boldsymbol{u}_2)^{\intercal}(\boldsymbol{u}_1 - \boldsymbol{u}_2) = \frac{4}{9} \tag{55}$$

Then, the optimal solution for the overmodulation stage is:

$$d_{1j}^{\star} = \text{mid}\left\{0, \frac{9}{4}(\boldsymbol{u}_1 - \boldsymbol{u}_2)^{\intercal}(\boldsymbol{u}_{unc} - \boldsymbol{u}_2), 1\right\} \tag{56a}$$

$$d_{2j}^{\star} = 1 - d_{1j} \tag{56b}$$

## 7. Inner optimisation problem

The objective of the inner optimisation loop is to compute an optimal common-mode signal $u_0^{\star}$ to balance the DC-link capacitors of the 3L-NPC converter. The strategy assumes that a PWM stage is used to synthesize the solution obtained from the outer optimisation loop. To this end, the optimal SS is mapped into a three-phase reference signal $\boldsymbol{D}_{abc} = [D_a\ D_b\ D_c]^{\intercal} \in [-1, 1]^3$ obtained as [22]:

$$\boldsymbol{D}_{abc} = d_1^{\star}\boldsymbol{u}_{abc,1}^{\star} + d_2^{\star}\boldsymbol{u}_{abc,2}^{\star} + \frac{1}{2}d_S^{\star}\left(\boldsymbol{u}_{abc,0}^{\star} + \boldsymbol{u}_{abc,3}^{\star}\right) \tag{57}$$

in which $\boldsymbol{u}_{abc,\ell}^{\star} = \mathbf{T}_{\alpha\beta}^{-1}\boldsymbol{u}_{s\ell}^{\star}$ are the three-phase switching states that produce the optimal SS. The optimal common-mode signal is the solution to the following optimisation problem:

$$u_o^{\star} = \min_{u_o}\ (v_n[k+1] - v_n^*)^2 \tag{58a}$$

$$\text{s.t.}\quad u_o[k] \in [-\Delta_o, \Delta_o] \tag{58b}$$

in which $v_n^*$ is the reference value of the DC-link NP-voltage, $v_n[k+1]$ is the discrete-time model of the NP voltage and $\Delta_o$ is a time-varying saturation level which represents the voltage available in the DC-link. The solution to the optimisation problem yields the following equation:

$$u_o^{\star} = \text{mid}\left\{-\Delta_o, -\frac{\alpha[k] - (v_n^* - v_n[k])}{\beta[k]}, \Delta_o\right\} \tag{59}$$

where $\alpha[k]$ and $\beta[k]$ are determined at each sampling instant according to:

$$\begin{aligned}\alpha[k] &= \frac{T_s}{C_1 + C_2}\sum_{x\in\mathcal{P}}|D_x|i_x \\ \beta[k] &= \frac{T_s}{C_1 + C_2}\sum_{x\in\mathcal{P}}\text{sgn}\{D_x\}i_x\end{aligned} \tag{60}$$

where $x \in \mathcal{P} = \{a, b, c\}$. The time-varying saturation level is defined as:

$$\Delta_o[k] = \min\{1 - |D_x[k]|\} \tag{61}$$

Finally, the three-phase reference signals sent to the PWM modulator are:

$$\boldsymbol{D}_{abc}^{\star} = \boldsymbol{D}_{abc} + u_0^{\star} \tag{62}$$

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For a more throughout explanation of the inner optimisation loop, the reader is referred to [22].

## 8. Hardware-in-the-Loop (HIL) Results

In this section, Hardware-in-the-Loop (HIL) results are shown to validate the proposed controller. The 3L-NPC converter, LC filter and loads are emulated using PLECS-RT box 1 HIL platforms with a time-step of 5 $\mu$s. The control system is separately implemented using a dSPACE MicroLabBox platform. This dSpace controller is equipped with a Freescale QorIQ P5020 dual-core 2 GHz processor, for number crunching, and a Kintex-7 XC7K325-T FPGA. The FPGA handles the AD conversion, performs an In-Phase Disposition PWM strategy and implements a dead time of 1 $\mu$s for each switching device; the HIL system is shown in Figure 5(a). The processor computes the Clark transform of the measured three-phase variables, executes the optimisation algorithm, and computes the appropriate three-phase reference signals for the modulator. The loads considered for the study are a three-phase resistive load bank and a nonlinear load implemented using a three-phase diode rectifier with a capacitor and resistor connected in parallel at the DC side, as shown in Figure 5(b). The parameters of the system are shown in Table 1 and are similar to those used in a previous work (see [23]).

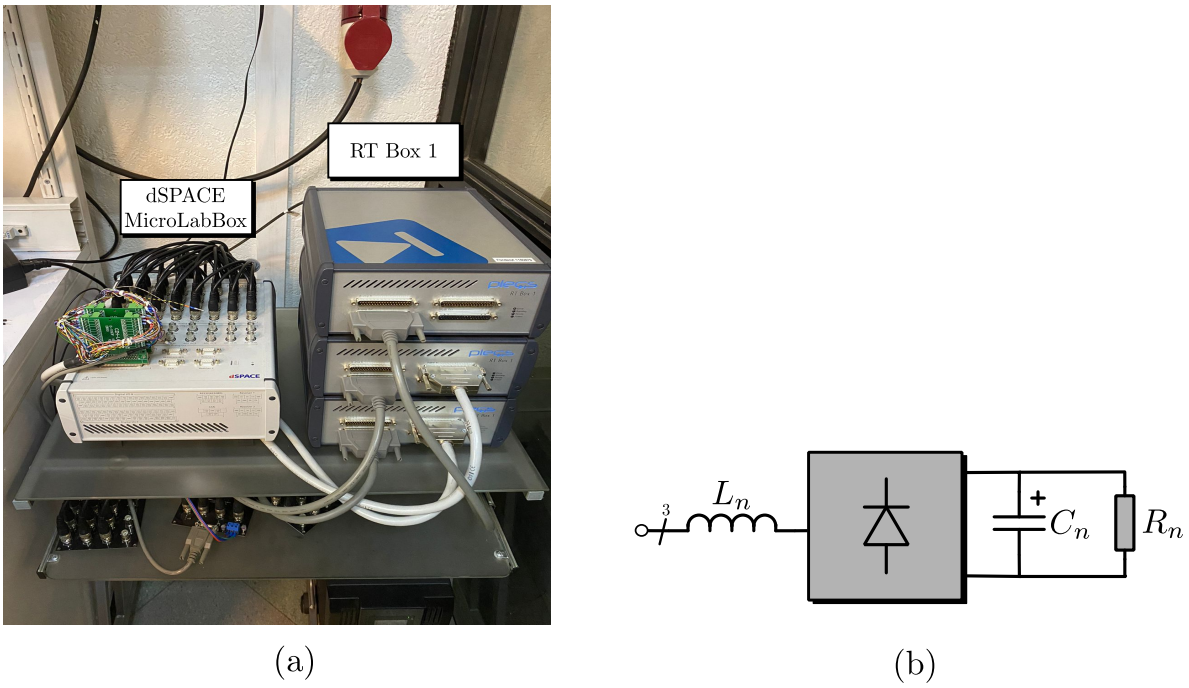


**Figure 5.** (a) HIL platform used to perform the experiments, and (b) topology of the nonlinear load.

**Table 1.** System Parameters.

| Parameter | Value |
|---|---|
| Switching and Sampling frequency | $f_s$ = 20 [kHz] |
| DC-link voltage | $V_{dc}$ = 700 V |
| LC Filter | $R_f$ = 1 m$\Omega$ $L_f$ = 2.4 mH $C_f$ = 15 $\mu$F |
| Load resistance | $R_L$ = 30 $\Omega$ |
| Non-linear load | $L_n$ = 1.8 mH $C_n$ = 2.2 mF $R_n$ = 60 $\Omega$ |
| Filter current weight factor | $\lambda_i$ = 0.25 |
| Load voltage weight factor | $\lambda_v$ = 0.02 |
| Control effort weight factor | $\lambda_u$ = 0 |

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The performance of the controllers is evaluated using the following goodness factors: RMS error (RMSE), percentage of voltage error ($E_v$) and total harmonic distortion (THD). The percentage of error is defined as follows:

$$E_v[\%] = \frac{100}{\|\boldsymbol{v}^*\|}\sqrt{\frac{1}{N_p}\sum_{k\in\mathcal{P}}\|\boldsymbol{v}(k)-\boldsymbol{v}^*(k)\|_2^2} \tag{63}$$

where $\mathcal{P} = \{1, 2, \ldots, N_p\}$ is the set of indices of the measurements vector, and $N_p = T_1/T_s$ is the total number of elements in the vector. $T_1$ is the period of the fundamental frequency, and $T_s$ is the period of the sampling frequency. Whenever the desired reference amplitude is unknown, the root-mean-square error (RMSE) will be used. The RMS error is defined as follows:

$$\text{RMSE}(\boldsymbol{x}-\boldsymbol{x}^*) = \sqrt{\frac{1}{N_p}\sum_{k\in\mathcal{P}}\|\boldsymbol{x}(k)-\boldsymbol{x}^*(k)\|_2^2} \tag{64}$$

A one-step delay compensation is carried out to compensate for the computational delay introduced by the digital platform. The state vector $\boldsymbol{x}_s[k+1]$ is computed using (20) with the values measured at the *kth* instant, and the switching sequence applied during the previous switching interval. The voltage reference $\boldsymbol{v}_o[k+1]$ is computed shifting the phase of the reference signal one step ahead. The load output current $\boldsymbol{i}_o[k+1]$ is estimated using the Lagrange extrapolation technique. The Lagrange extrapolation technique uses the actual and past measurements of the signal to estimate its future value. The load output current $\boldsymbol{i}_o[k+1]$ is computed as follows [37]:

$$\boldsymbol{i}_o[k+1] = 4\boldsymbol{i}_o[k] - 6\boldsymbol{i}_o[k-1] + 4\boldsymbol{i}_o[k-2] - \boldsymbol{i}_o[k-3] \tag{65}$$

The estimated load output current has an RMS error of 0.0603 [A] in the $\alpha$-component, and 0.0640 [A] in the $\beta$-component for the worst-case scenario (nonlinear load). The estimated and measured load output current are shown in Figure 6. As shown in this figure, the estimated current tracks relatively well the measured current.

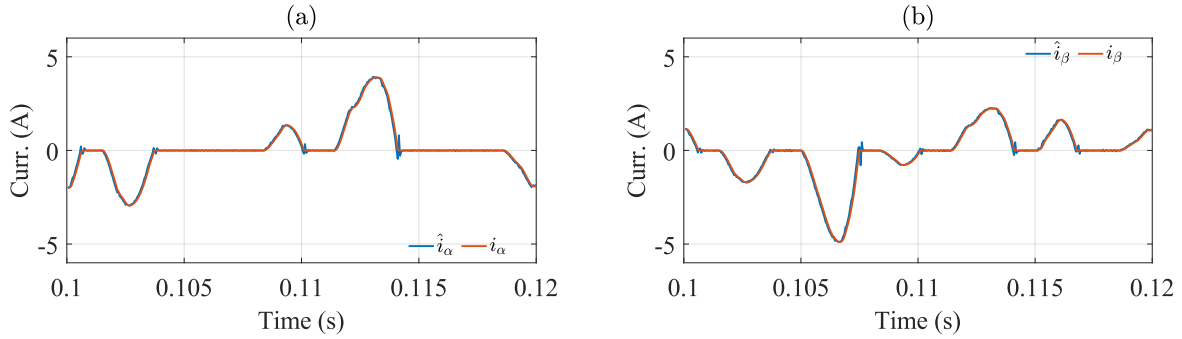


**Figure 6.** Estimated and measured current when a nonlinear load is connected. (a) $\alpha$-component of the load current, and (b) $\beta$-component of the load current.

In Figure 7(a), the output voltages when the system operates without load are shown. The reference voltage has an amplitude of 300 [V] with a frequency of 50[Hz]. For this condition, the load output voltages have a voltage error of 2.04% and a THD of 1.74%. Then, a three-phase resistive load is connected as in Figure 7(d). In this condition, the voltage error is 2.05% and the THD is 1.03%. When a nonlinear load is connected, as in Figure 7(g), the voltage error is 2.83%. The harmonic spectrum for the load output voltage and load output current are shown in Figure 8(a)-(b). The voltage THD in this case is 2.73% with the presence of 5th and 7th harmonics, which are produced by the bridge rectifier. In Figure 7(b)-(h) the load output current is shown for the three aforementioned cases. Finally, in Figure 7(c)-(i), the DC-link capacitor voltages are shown. The control strategy is capable of maintaining the DC-link voltages balanced and well regulated, for all operating conditions with very small oscillations.

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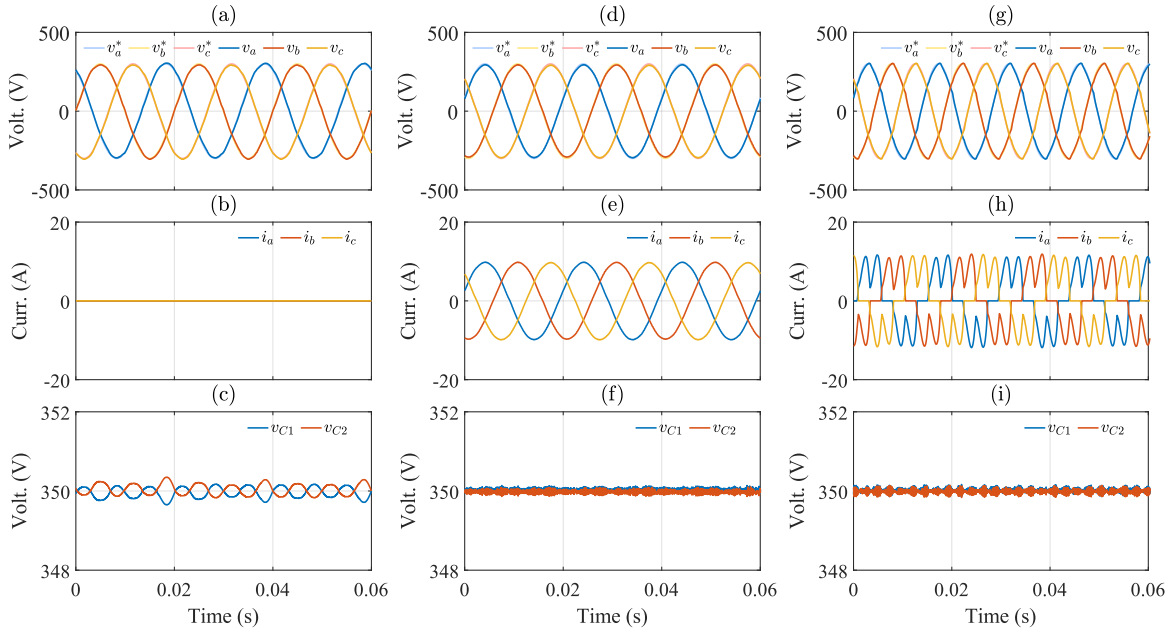


**Figure 7.** Steady-state results for different load conditions. (a,d,g) Load output voltage without load, with resistive load and with nonlinear load, (b,e,h) load output current without load, with resistive load and with nonlinear load, and (c,f,i) DC-link capacitor voltages without load, with a resistive linear load and nonlinear load.

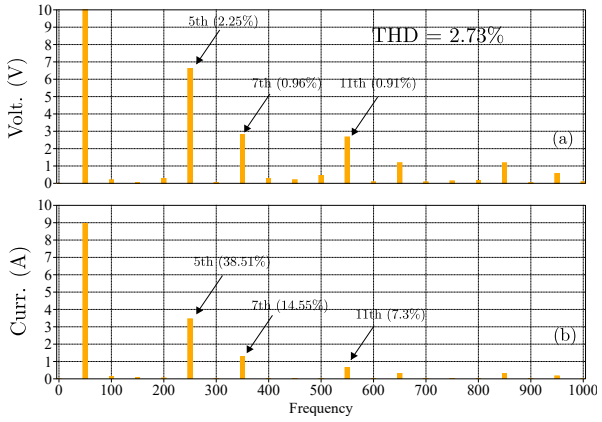


**Figure 8.** Harmonic spectrum of (a) load output voltage, and (b) load output current when a nonlinear load is connected.

The transient operation of the controlled system is studied in Figure 9 considering changes in the reference voltage amplitude. The variables are presented in the synchronous reference frame to verify the settling time of the load output voltage.

The settling time is computed as the time required by the output voltage to reach and stay within 5% of the desired voltage. In Figure 9(a) the reference voltage receives a step variation from 300 [V] to 100 [V] at t = 0.2 [s]. The voltage error amounts to 5.98% under steady-state conditions. The rise in voltage error results from the reduction in the amplitude of the reference voltage. In Figure 9(b), the reference voltage varies from 100 [V] to 300 [V] at t = 0.2 [s]. In this case, the load output voltage manages to stay within the band of 5% around the desired voltage. Thus, the settling time is 1.03 [ms] approximately.

Notice that a relatively low steady-state error is presented in the HIL results shown in Figure 9 *a* and *b*. This small steady-state error is produced because there is not an integrator in the MPC algorithm [38,39]. If steady state error is a must, then the state space matrix $\boldsymbol{A}$ [see (7)] must be

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augmented with additional states to represent the integrator [38]; however, this topic is considered outside the scope of this work.

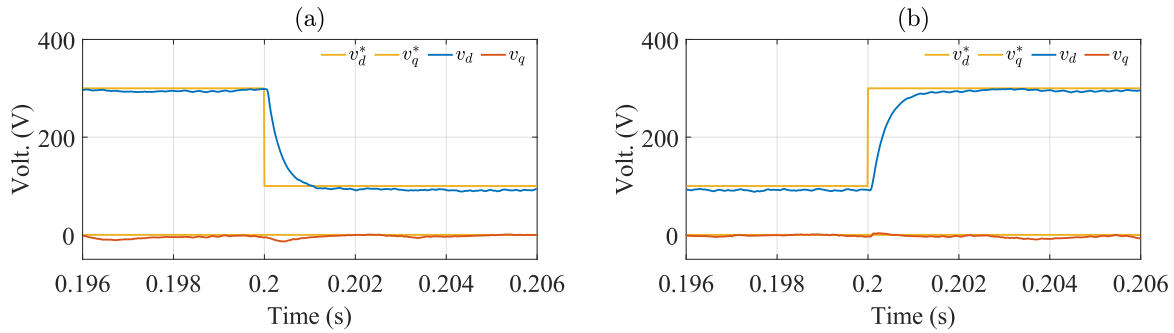


**Figure 9.** Transient operation of the system for reference voltage step. (a) voltage step from 300 [V] to 100 [V], (b) voltage step from 100 [V] to 300 [V].

Figure 10 shows the operation of the system for a load step. A dip occurs in the load output voltage, as shown in Figure 10(a), and takes 1 [ms] approximately to recover. Notice that there is a sudden increase in the inductor reference current to 10 A approximately, and the current features a fast dynamic response to the step change.

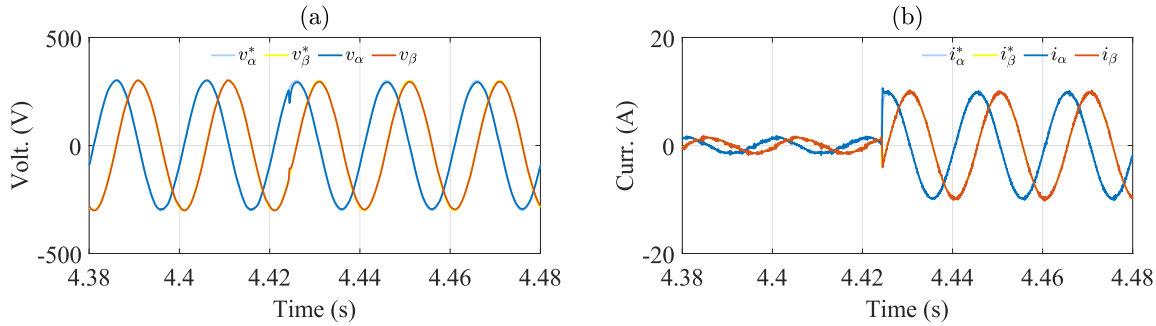


**Figure 10.** Transient operation of the system for a load step. (a) Load output voltage, and (b) Filter inductor current.

The cost function of (30) has two terms: the first term penalizes the deviation of the system states from a reference vector and the second term penalizes the control effort of the converter. The control effort is penalized in the cost function by the deviation between the optimisation variable $\boldsymbol{u}(k)$ and the steady-state control action $\boldsymbol{u}_{ss}$. The weight of this deviation on the optimisation problem is set by the parameter $\lambda_u$. Increasing $\lambda_u$ will lead the converter's response to move closer to open-loop operation since $\boldsymbol{u}_s s$ depends only on the load reference voltage and load output current. The system's performance with a logarithmic variation of the parameter $\lambda_u$ is shown in Figure 11. The results are obtained considering a three-phase resistive load at the LC filter terminals. The best trade-off in terms of voltage error between open-loop and closed-loop operation of the converter is achieved when $\lambda_u = 10$, as shown in Figure 11(a). When $\lambda_u$ is increased, the response of the system tends toward $\boldsymbol{u}_{ss}$ which does not penalize the voltage error. Thus, the voltage error increases.

As shown in Figure 11(b), the voltage THD presents slight variations around 1%, as shown in Figure 11(b). The system's transient response is also dependent on the value of $\lambda_u$. A trade-off between settling time and overshoot must be reached, as shown in Figure 12. Increasing $\lambda_u$ up to 100 will reduce the settling time of the system but increase the voltage overshoot. However, for $\lambda_u >> 100$, the system response will present a damped sinusoidal oscillation which increases the settling time.

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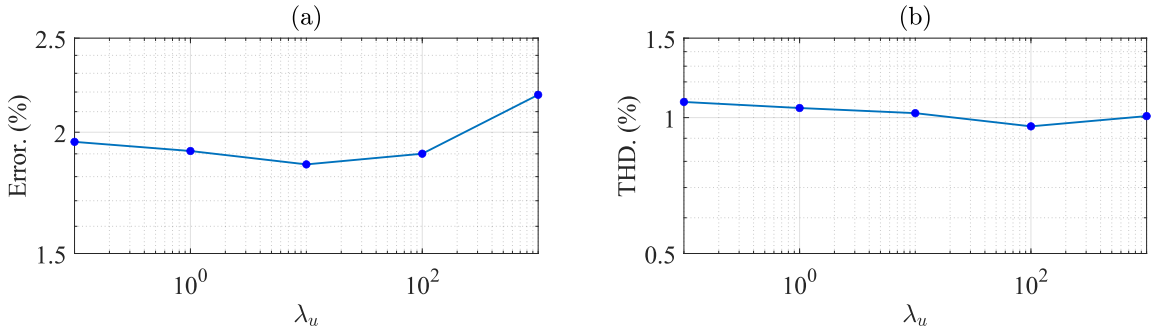


**Figure 11.** System performance over variation of $\lambda_u$.

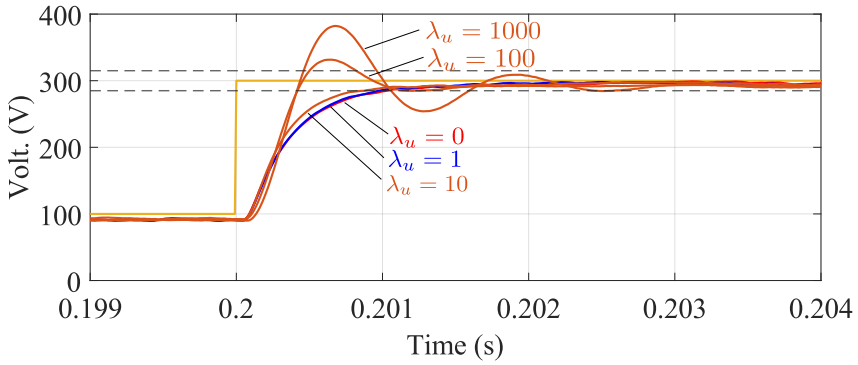


**Figure 12.** Transient operation of the system for different values of $\lambda_u$.

## 9. Conclusions

In this paper, an Optimal Switching Sequence MPC algorithm was proposed for the three-level neutral-point-clamped inverter with an output LC filter. The strategy is an extension of the Cascaded Optimal Switching Sequence MPC proposed in the literature for current and direct power control of active front-end 3L-NPC inverters. The control objectives of the algorithm were two: (1) achieve good tracking performance for the LC filter variables, and (2) maintain balanced the neutral-point voltage between the DC-link capacitors of the converter. To achieve the objectives, the strategy solves two cascaded optimisation problems. The first optimisation problem -called the outer optimisation loop- computes the optimal sequence of switching vectors and their corresponding duty cycles to achieve the objectives related to tracking the AC side variables. Then, the optimal solution of the outer optimisation loop is used by an inner optimisation loop to compute an optimal common-mode signal designed to balance the neutral-point voltage between the DC-link capacitors. A discrete-time model based on the improved Euler discretization method was used to predict the future values of the state vector trajectory. Notice that this methodology allows the implementation of a single-stage MPC algorithm to regulate the load voltage and the converter output current.

Experimental results are provided to validate the performance of the proposed strategy using PLEXIM Hardware-in-the-Loop (HIL) platform RT Box 1 to emulate the power electronics stage, and the control algorithm was executed by the dSPACE MicroLabBox control platform. Three cases were considered in steady-state operation: (1) system performance without load, (2) system performance with linear load, and (3) system performance with nonlinear load. In all cases, the MPC algorithm is capable of achieving good tracking of the load voltage reference with a small error and low THD. Also, the strategy is capable of maintaining well-balanced voltages at the DC-link capacitors.

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Resources, Matías Díaz; Software, Felipe Herrera, Matías Díaz and Marco Rivera; Supervision, Andrés Mora and Roberto Cárdenas; Validation, Felipe Herrera, Andrés Mora and Roberto Cárdenas; Writing – original draft, Felipe Herrera and Andrés Mora; Writing – review & editing, Andrés Mora, Roberto Cárdenas, Matías Díaz, Jose Rodriguez and Marco Rivera. All authors have read and agreed to the published version of the manuscript.

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## Abbreviations

The following abbreviations are used in this manuscript:

| | |
|---|---|
| 7S-SS | Seven Segments Switching Sequence |
| DC | Direct Current |
| AC | Alternate Current |
| FPGA | Field Programmable Gate Array |
| FCS-MPC | Finite Control Set Model Predictive Control |
| $M^2PC$ | Modulated Model Predictive Control |
| HIL | Hardware in the Loop |
| LC-filter | Inductance Capacitor Filter |
| MIMO | Multiple-Input Multiple-Output |
| MPC | Model Predictive Control |
| NPC | Neutral Point Clamped |
| OSS | Optimal Switching Sequence |
| OSV | Optimal Switching Vector |
| PWM | Pulse Width Modulation |
| RT | Real Time |
| SISO | Single-Input Single-Output |
| THD | Total Harmonic Distortion |
| UPS | Uninterruptible Power Supply |
| VFD | Variable Frequency Drives |

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