0.5-V 281-nW Versatile Mixed-Mode Filter Using Multiple-InPut/Output Differential Difference Transconductance Amplifiers

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Article

0.5-V 281-nW Versatile Mixed-Mode Filter Using Multiple-Input/Output Differential Difference Transconductance Amplifiers

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Abstract: This paper presents a new low-voltage versatile mixed-mode filter which uses a multiple-input/output differential difference transconductance amplifier (MIMO-DDTA). The multiple-input of the DDTA is realized using a multiple-input bulk-driven MOS transistor (MI-BD-MOST) technique to maintain a single differential pair, thereby achieving simple structure with minimal power consumption. In a single topology, the proposed filter can provide five standard filtering functions (low-pass, high-pass, band-pass, band-stop, and all-pass) in four modes: voltage (VM), current (CM), transadmittance (TAM), and transimpedance (TIM). This provides the full capability of a mixed mode filter (i.e., twenty filter functions). Moreover, the VM filter offers high-input and low-output impedances and the CM filter offers high-output impedance; therefore, no buffer circuit is needed. The natural frequency of all filtering functions can be electronically controlled by a setting current. The voltage supply is 0.5 V and for a 4 nA setting current, the power consumption of the filter was 281 nW. The filter is suitable for low-frequency biomedical and sensor applications that require extremely low supply voltages and nano-watt power consumption. For the VM low-pass filter, the dynamic range was 58.23 dB @ 1 % total harmonic distortion. The proposed filter was designed and simulated in the Cadence Virtuoso System Design Platform using the 0.18 μm TSMC CMOS technology.

Keywords: Universal filter; mixed-mode filter; differential difference transconductance amplifier; operational transconductance amplifier

1. Introduction

Active analog blocks, such as the operational amplifier (OA) or the transconductance amplifier (TA), are essential components for electronic devices, communication systems, and sensor interfaces. These blocks typically use the standard two inputs (i.e., a single differential stage). However, it has been confirmed that the use of a block with multiple inputs can reduce the number of components, silicon area, and power dissipation of some applications by a factor of approximately k, where k is the number of TA inputs [1]. Several applications based on this concept have been presented in [1–4]. Some other examples of multiple-input blocks are the differential difference amplifier (DDA) [5–9], differential difference current conveyor (DDCC) [10,11], differential difference operational floating amplifier (DDOFA) [12], differential difference transconductance amplifier (DDTA) [13,14], and many others. All these blocks allow for more arithmetic operations due to their multiple-input character and are therefore widely used in instrumentation amplifiers, signal conditioning, differential amplification, filters, and many other applications. Although these blocks can reduce an application's complexity and the number of blocks utilized, their internal structure is more complex than that of a standard two-input block. This is primarily due to the increased number of differential stages that are required to increase the number of inputs. The multiple-input MOS transistor (MI-MOST) provides a solution to avoid this problem and maintain a single differential stage [15–17]. It can be used in any standard CMOS technology without constraints. The first experimental results of MI-MOST were presented in [15–17] and various applications based on it were presented in [18–29].

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Filters play an important role in electronic, telecommunication and control systems. They can be used to reduce harmonics and filter noise in an electronic system, to separate or select desired signals, to remove unwanted signals in telecommunication systems, or to reduce the noise component of measurement signals in a control system. There are five common filtering functions that can be classified, namely the low-pass filter (LPF), high-pass filter (HPF), band-pass filter (BPF), band-stop filter (BSF), and all-pass filter (APF). These filtering functions can be designed using passive and active components, called passive filters or active filters, respectively. Second-order filters (or biquad filters) can be used to realize high-order filters applied to a high-fidelity three-ways crossover loudspeaker network and to a phase-locked loop.

Using active device-based filters, second-order LPF, HPF, BPF, BSF and APF (five filter functions) can be provided in a single topology, creating the so-called universal filter. Circuits that can provide voltage-mode (VM) (input and output as voltage), current-mode (CM) (input and output as current), transadmittance-mode (TAM) (input as voltage and output as current) and transimpedance-mode (TIM) (input as current and output as voltage) transfer functions in the same circuit are classified as mixed-mode universal filters. In a perfect mixed-mode universal filter, each mode of the transfer function should provide five filter functions, therefore obtaining twenty filter functions in a single topology. In addition, perfect universal filters should have high input impedance and low output impedance if the input and output are in voltage forms and low input and high output impedance if the input and output are in current forms.

There are many mixed-mode universal filters available in open literature [30–67]. The circuits in [30–43] realize a mixed-mode universal filter using variant active devices such as current conveyors [30–39], the CFOA (current feedback operational amplifier) [40–42], the FTFN (four terminal floating nullor) [43]; however, these filters lack electronic tuning capabilities. The circuits in [44–46] use current-controlled current conveyors-based filters to offer electronic tuning capability, but the circuits in [44,45,47] do not provide twenty transfer functions and the circuits in [46,47] require input matching conditions.

To obtain electronic tuning capability, the circuits in [48–51] use the CCTA (current conveyor transconductance amplifier), the circuit in [52] uses the VDTA (voltage differencing transconductance amplifier), the circuits in [53,54] use the VD-DVCC (voltage differencing differential voltage current conveyor), and the circuits in [55,56] use the VDBA (voltage differencing buffered amplifier). However, the circuits in [48,51,52] do not offer twenty transfer functions, the circuits in [53,54] require active/passive component matching conditions, and the circuits in [55,56] apply input voltage signals via a passive capacitor and/or resistor.

The OTA (operational transconductance amplifier) has been used to realize mixed-mode universal filters [57–66]. However, the circuits in [57,59,65] require passive or active components, the circuits in [58,61–63] do not provide twenty transfer functions, and the circuits in [57,58,64,66] require inverted input signals. It should be noted that the structure of active devices used in [30–66] is not designed for low-voltage low-power filters. Filters for such applications are in high demand especially for biosignals and sensors signal processing. Many filters based on multiple-input DDTA have been presented [67–74].

This paper presents a versatile mixed-mode filter using MIMO-DDTAs. The circuit has six input voltages, three input currents, three output voltages, and two output currents; as such, it offers 61 transfer functions of LPF, BPF, HPF, BSF, and APF in the same topology. The six input voltage terminals possess a high-impedance level, and the three output voltage nodes possess a low-impedance level which is ideal for voltage-mode circuits. The two output current terminals also possess a high-impedance level which can be connected directly to loads without buffer circuit requirements. The natural frequency of the filters can also be controlled electronically. The proposed versatile mixed-mode filter uses a supply voltage of 0.5 V and 281 nW of power consumption.

The paper is organized as follows: Section 2 describes the multiple-input/output DDTA. Section 3 describes the application of the versatile mixed-mode filter and non-ideality analysis. Sections 4 presents the simulation results. Finally, the conclusion is given in Section 5.

2. Proposed DDTA Circuit with Multiple-Input and Multiple-Output

The electrical symbol of the proposed multiple-input/output differential-difference transconductance amplifier is shown in Figure 1. Its performance, in an ideal case, is described by Eqn. (1). The circuit possesses one low-impedance output w, which provides a difference of the sums of the voltages V_{y+} and V_{y-}, applied to its non-inverting and inverting terminals, respectively. It further has a high-impedance output o, which provides a current, proportional to the voltage V_w appearing at the w terminal.

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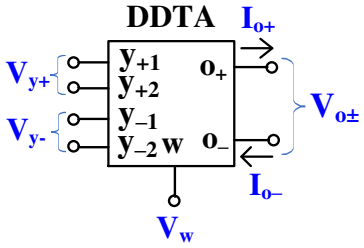

Figure 1. Electrical symbol of the MIMO-DDTA.

$$\left.\begin{aligned} V_w &= V_{y+1} + V_{y+2} - V_{y-1} - V_{y-2} \\ I_{o\pm} &= \pm g_m V_w \end{aligned}\right\} \quad (1)$$

The CMOS structure of the proposed circuit is shown in Figure 2. The circuit consists of two blocks, a multiple-input differential-difference amplifier (MI-DDA) and a multiple-output transconductance amplifier (MO-TA).

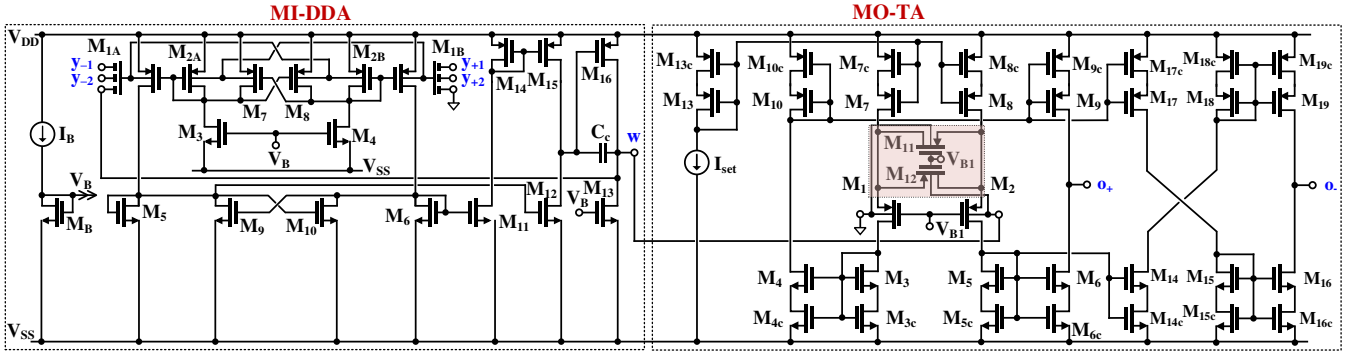

Figure 2. CMOS structure of the MIMO-DDTA.

The MI-DDA can be seen as a two-stage internal OTA, operating in a unity-gain feedback configuration. The first gain stage is formed by the transistors M_1-M_{12}, M_{14}, M_{15}, while the second stage is formed by the transistors M_{13} and M_{16}. The capacitance C_C is used for frequency compensation. The first stage can be seen as a current-mirror OTA, with a differential amplifier M_1-M_{10} and a set of current mirrors M_5-M_{12}, M_6-M_{11}, M_{14}-M_{15}, acting as a differential to single output converter.

The input stage is based on a non-tailed bulk-driven differential pair M_1-M_4, which behaves as a differential amplifier with high CMRR and PSRR performances, while also being able to operate at extremely low supply voltages [75], even lower than the threshold-voltages of the used MOS transistors. In order to increase the voltage gain, a partial positive feedback (PPF) is applied. The PPF is created by two cross-coupled transistor pairs: M_7-M_8 and M_9-M_{10}. The cross-coupled pairs generate negative conductances that partially compensate the conductances of the diode-connected transistors $M_{2A,B}$ for the "upper" pair, and M_5, M_6 for the "lower" pair. Therefore, the resulting conductances increase at the drains of these transistors, and consequently, the first stage transconductance and voltage gain also increase. In particular, the upper pair increases the voltage gain from the bulk terminals to the gates of $M_{1A,B}$ [76], while the lower pair increases the current gains of the current mirrors M_5-M_{12} and M_6-M_{11} [77]. The combination of two PPF circuits decreases the overall sensitivity of the transconductance gain of the first stage to transistor mismatch [69]. This achieves a larger voltage gain while maintaining relatively low sensitivity of the input stage and avoiding problems with frequency compensation of the DDA.

In order to realize a differential to difference function without duplicating the input stage, the multiple inputs were realized using the so-called multiple-input BD MOS transistors [15]. The symbol and the implementation of the devices are shown in Figs.3a and 3b, respectively. A passive capacitive voltage divider is applied to the bulk terminal of the MOS transistor, thus creating a multiple-input device. The large resistors R_{MOSi}, used to bias the bulk terminal for DC, are realized using two minimum-size MOS transistors operating in a cut-off region, as shown in Figure3c.

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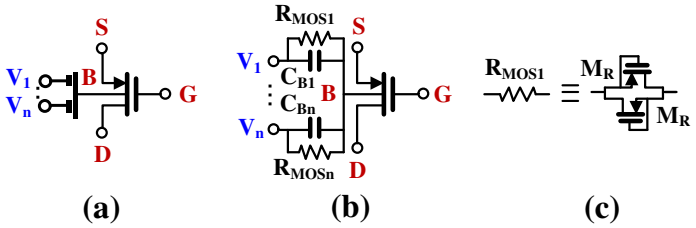

Figure 3. MI-BD MOST: (a) symbol, (b) possible implementation, (c) implementation of R_{MOS}.

Assuming $1/\omega C_{Bi} \ll R_{MOSi}$, the voltage V_b at the bulk terminal of the MI-BD-MOS transistor can be expressed as:

$$V_b = \sum_{i=1}^{n} \beta_i V_i \tag{2}$$

where n is the number of inputs and β_i is the voltage gain of the input capacitive divider:

$$\beta_i = \frac{C_{Bi}}{\sum_{i=1}^{n} C_{Bi}} \tag{3}$$

Note that with equal C_{Bi}, $\beta_i = 1/n$.

The open-loop voltage gain of the DDA can be expressed as:

$$A_{vo} = \beta \frac{2g_{mb1}(r_{ds15}||r_{ds12})g_{m16}(r_{ds16}||r_{ds13})}{(1-m_1)(1-m_2)} \tag{4}$$

where the coefficients m_1 and m_2 are the ratios of the absolute values of the negative and positive conductances in a lower and upper PPF circuit, respectively [68]:

$$m_1 = \frac{g_{m9,10}}{g_{m5,6}+g_{ds2}+g_{ds3,4}+g_{ds7,8}} \cong \frac{g_{m9,10}}{g_{m5,6}} \tag{5}$$

$$m_2 = \frac{g_{m7,8}}{g_{m2}+g_{ds1}+g_{ds5,6}+g_{ds9,10}} \cong \frac{g_{m7,8}}{g_{m2}} \tag{6}$$

Note that the above coefficients should always be lower than unity to maintain circuit stability. In the proposed design, $m_1=m_2=0.5$. This increased the voltage gain by 12 dB, thus compensating the gain loss introduced by the input capacitive divider (approximately 10 dB) while maintaining the overall circuit sensitivity to transistor mismatch at a relatively low level.

The second block creating the MIMO-DDTA is the multiple output transconductance amplifier. The circuit can be seen as a current-mirror linear OTA. Note that a version of the MI-TA with one positive output was presented and verified experimentally in [18]. Here, a second, inverting output has been added, thus increasing the circuit universality. Transistors M_1, M_2 and M_{11}, M_{12} realize an input differential stage. The transistors M_{11} and M_{12} operate in a triode region and extend the linear range of the structure. The circuit can be seen as a BD version of the Krummenacher and Joehl transconductor [78], operating in weak inversion. Thanks to the BD approach, the linear range of the circuit is extended $\eta=g_{m1,2}/g_{mb1,2}$ times, as compared with its gate-driven (GD) counterpart. In order to obtain optimum linearity, the following condition should be met [18]:

$$k = \frac{(W/L)_{11,12}}{(W/L)_{1,2}} = 0.5 \tag{7}$$

where W and L is the MOS transistor channel width and length, respectively.

Assuming unity current gain of all current mirrors, the circuit transconductance is given by:

$$g_m = \eta \frac{4k}{4k+1} \cdot \frac{I_{set}}{n_p U_T} \tag{8}$$

where n_p is the subthreshold slope factor, U_T is the thermal potential and I_{set} is the biasing current. Note that the circuit transconductance is proportional to this current.

In order to increase the DC voltage gain of the structure while not limiting its output voltage range, all current mirrors are based on self-cascode transistors. Consequently, the DC voltage gain from the input to the differential output is equal to:

$$A_{VO} \cong 2g_m[(g_{m9}r_{ds9}r_{ds9c})||(g_{m6}r_{ds6}r_{ds6c})] \tag{9}$$

Thanks to the self-cascode technique, it is possible to compensate for the gain loss associated with the application of the BD technique. In practice, a voltage gain of around 40 dB can be obtained.

3. Versatile Mixed-Mode Filter

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Figure 4 shows the proposed versatile mixed-mode universal filter employing four MIMO-DDTAs and two grounded capacitors. Using (1) and nodal analysis, the output voltages V_{o1}, V_{o2}, V_{o3} and the output currents I_{o1}, I_{o2} can be given by:

$$V_{o1} = \frac{g_{m3}}{g_{m4}} \cdot \frac{s^2C_1C_2(V_5-V_6)+sC_1g_{m2}(V_3-V_4)+g_{m1}g_{m2}(V_1-V_2)}{s^2C_1C_2+sC_1g_{m3}+g_{m2}g_{m3}} \quad (10)$$

$$V_{o2} = \frac{s^2C_1C_2(V_5-V_6)+sC_1g_{m2}(V_3-V_4)+g_{m1}g_{m2}(V_1-V_2)}{s^2C_1C_2+sC_1g_{m3}+g_{m2}g_{m3}} \quad (11)$$

$$V_{o3} = \frac{sC_2g_{m3}(V_5-V_6)+(s^2C_1C_2+sC_2g_{m3})(V_3-V_4)+(sC_2g_{m3}+g_{m1}g_{m3})(V_1-V_2)}{s^2C_1C_2+sC_1g_{m3}+g_{m2}g_{m3}} \quad (12)$$

$$I_{o1} = g_{m3} \cdot \frac{s^2C_1C_2(V_5-V_6)+sC_1g_{m2}(V_3-V_4)+g_{m1}g_{m2}(V_1-V_2)}{s^2C_1C_2+sC_1g_{m3}+g_{m2}g_{m3}} \quad (13)$$

$$I_{o1} = \frac{-s^2C_1C_2I_3+sC_1g_{m3}I_2-g_{m2}g_{m3}I_1}{s^2C_1C_2+sC_1g_{m3}+g_{m2}g_{m3}} \quad (14)$$

$$I_{o2} = \frac{s^2C_1C_2I_3-sC_1g_{m3}I_2+g_{m2}g_{m3}I_1}{s^2C_1C_2+sC_1g_{m3}+g_{m2}g_{m3}} \quad (15)$$

$$V_{o1} = \frac{1}{g_{m4}} \cdot \frac{-s^2C_1C_2I_3+sC_1g_{m3}I_2-g_{m2}g_{m3}I_1}{s^2C_1C_2+sC_1g_{m3}+g_{m2}g_{m3}} \quad (16)$$

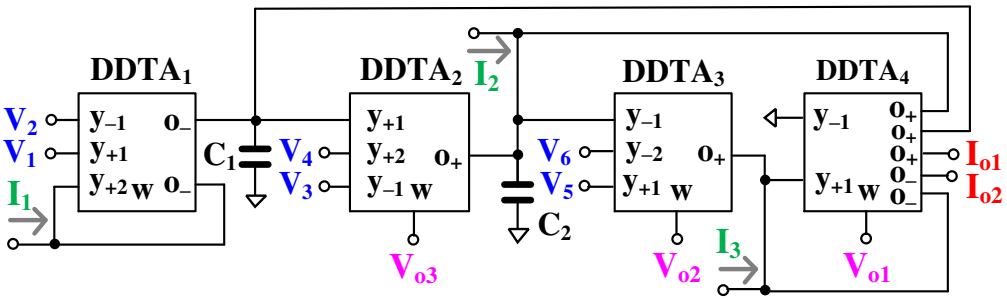

Figure 4. The proposed versatile mixed-mode filter using MIMO-DDTAs.

From (10)-(16), the variant filtering functions can be determined and are shown in Table 1. The proposed mixed-mode universal filter can offer LP, HP, BP, BS, and AP filtering functions of VM, CM, TAM, and TIM in the same topology. Thanks to the multiple inputs of the DDTA, the VM, CM, and TIM can offer non-inverting and inverting transfer functions of LP, HP, BP, BS, and AP filters, and the VM and TAM can also offer differential transfer functions of LP, HP, BP, BS, and AP filters. Thus, the proposed mixed-mode filter can provide 61 transfer functions in a single topology. Thanks to the multiple outputs of the DDTA, such as DDTA4, the proposed filter utilizes a minimum number of used DDTAs while offering inverting and non-inverting transfer functions of LP, HP, BP, BS, and AP filters of CM. The input signals V_1 to V_6 are connected to the high-impedance terminals of the DDTA; thus, the voltage signals can be applied without any buffer circuit requirements. The output signals V_{o1} to V_{o3} are connected to the low-impedance terminals of the DDTA, which offers a cascadable output for the voltage-mode filter structures. The output signals I_{o1} and I_{o2} are connected to the high-impedance terminals of the DDTA, which offers a cascadable output for the current-mode filter structures. However, in the case of CM, the inputs I_1 to I_3 require additional circuits, such as multiple-output current followers or multiple-output current mirrors, to create three identical current signals from the single original current signal. It is clear that the proposed filter is exempt from inverting-type input signal and input matching conditions for realizing all filtering functions both in the case of voltage and current signals.

The voltage gain g_{m3}/g_{m4} of the filtering functions can be obtained if the output V_{o1} is used. In the case of TAM, the inputs V_1 to V_6 are converted to output currents by g_{m3}; in the case of TIM, the input currents I_1 to I_3 are converted to output voltages by g_{m4}.

The natural frequency (ω_o) and the quality factor (Q) can be given by:

$$\omega_o = \sqrt{\frac{g_{m2}g_{m3}}{C_1C_2}} \quad (17)$$

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$$Q = \sqrt{\frac{C_2 g_{m2}}{C_1 g_{m3}}} \tag{18}$$

It should be noted that the parameter ω_o can be controlled electronically by g_{m2} and g_{m3} and the parameter Q can be given by C_2/C_1.

TABLE I. Obtaining variant filtering functions of the proposed versatile mixed-mode filter.

Operation mode	Filtering Function		Input	Output
VM	LP	Non-inverting	V_1	V_{o1}
		Inverting	V_2	V_{o1}
		Non-inverting	V_1	V_{o2}
		Inverting	V_2	V_{o2}
		Non-inverting	$V_1 = V_6$	V_{o3}
		Inverting	$V_2 = V_5$	V_{o3}
		Differential	$V_1 - V_2$	V_{o2}
	BP	Non-inverting	V_3	V_{o1}
		Inverting	V_4	V_{o1}
		Non-inverting	V_3	V_{o2}
		Inverting	V_4	V_{o2}
		Non-inverting	V_5	V_{o3}
		Inverting	V_6	V_{o3}
		Differential	$V_3 - V_4$	V_{o2}
	HP	Non-inverting	V_5	V_{o1}
		Inverting	V_6	V_{o1}
		Non-inverting	V_5	V_{o2}
		Inverting	V_6	V_{o2}
		Non-inverting	$V_3 = V_6$	V_{o3}
		Inverting	$V_4 = V_5$	V_{o3}
		Differential	$V_5 - V_6$	V_{o2}
	BS	Non-inverting	$V_1 = V_5$	V_{o1}
		Inverting	$V_2 = V_6$	V_{o1}
		Non-inverting	$V_1 = V_5$	V_{o2}
		Inverting	$V_2 = V_6$	V_{o2}
		Differential	$(V_1 = V_5) - (V_2 = V_6)$	V_{o2}
	AP	Non-inverting	$V_1 = V_4 = V_5$	V_{o1}
		Inverting	$V_2 = V_3 = V_6$	V_{o1}
		Non-inverting	$V_1 = V_4 = V_5$	V_{o2}
		Inverting	$V_2 = V_3 = V_6$	V_{o2}
		Differential	$(V_1 = V_4 = V_5) - (V_2 = V_3 = V_6)$	V_{o2}
CM	LP	Non-inverting	I_1	I_{o1}
		Inverting	I_1	I_{o2}
	BP	Non-inverting	I_2	I_{o2}
		Inverting	I_2	I_{o1}
	HP	Non-inverting	I_3	I_{o1}
		Inverting	I_3	I_{o2}
	BS	Non-inverting	$I_1 = I_3$	I_{o1}
		Inverting	$I_1 = I_3$	I_{o2}
	AP	Non-inverting	$I_1 = I_2 = I_3$	I_{o1}
		Inverting	$I_1 = I_2 = I_3$	I_{o2}
TAM	LP	Non-inverting	V_1	I_{o1}
		Inverting	V_2	I_{o1}
		Differential	$V_1 - V_2$	I_{o1}
	BP	Non-inverting	V_3	I_{o1}
		Inverting	V_4	I_{o1}
		Differential	$V_3 - V_4$	I_{o1}
	HP	Non-inverting	V_5	I_{o1}
		Inverting	V_6	I_{o1}

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		Differential	V_5-V_6	I_{o1}
	BS	Non-inverting	$V_1=V_5$	I_{o1}
		Inverting	$V_2=V_6$	I_{o1}
		Differential	$(V_1=V_5)-(V_2=V_6)$	I_{o1}
	AP	Non-inverting	$V_1=V_4=V_5$	I_{o1}
		Inverting	$V_2=V_3=V_6$	I_{o1}
		Differential	$(V_1=V_4=V_5)-(V_2=V_3=V_6)$	I_{o1}
TIM	LP	Non-inverting	I_1	V_{o1}
	BP	Inverting	I_2	V_{o1}
	HP	Non-inverting	I_3	V_{o1}
	BS	Non-inverting	$I_1=I_3$	V_{o1}
	AP	Non-inverting	$I_1=I_2=I_3$	V_{o1}

3.1. Non-Ideality Analysis

Taking the tracking errors and the non-ideal transconductance of the MIMO-DDTA into account, the characteristics of the MIMO-DDTA can be rewritten as:

$$\left.\begin{matrix} V_w=\alpha_{j+}V_{y+1}+\alpha_{j+}V_{y+2}-\alpha_{j-}V_{y-}+\alpha_{j-}V_{y-2} \\ I_o=g_{mnj}V_w \end{matrix}\right\} \quad (19)$$

where α_{j+}=1-ε_{j+v} and ε_{j+v} ($|\varepsilon_{j+v}|\ll1$) denote the voltage tracking error from non-inverting terminals (i.e., V_{y+1}, V_{y+2}) to the w-terminal (i.e., V_w) of the j-th DDTA, α_{j-}=1-ε_{j-v} and ε_{j-v} ($|\varepsilon_{j-v}|\ll1$) denote the voltage tracking error from inverting terminals (i.e., V_{y-1}, V_{y-2}) to the w-terminal (i.e., V_w) of the j-th DDTA, and g_{mnj} is the non-ideal transconductance gain of the j-th DDTA. The non-ideal transconductance g_{mnj} of the j-th DDTA at a frequency near the cut-off frequency can be expressed by [65]:

$$g_{mnj}(s)\cong g_{mj}(1-\mu_j s) \quad (20)$$

where $\mu_j=1/\omega_{gmj}$, ω_{gmj} denotes the first pole frequency of the j-th g_m.

Using (19), the denominator of (10)-(16) can be modified as:

$$s^2C_1C_2+sC_1g_{mn3}\alpha_{3-}+g_{mn2}g_{mn3}\alpha_{2+}\alpha_{3-} \quad (21)$$

Using (20), (21) becomes:

$$\left\{s^2C_1C_2\left(1-\frac{C_1g_{m3}\mu_3\alpha_{3-}-g_{m2}g_{m3}\alpha_{2+}\alpha_{3-}\mu_2\mu_3}{C_1C_2}\right)+sC_1g_{m3}\alpha_{3-}\left(1-\frac{g_{m2}g_{m3}\alpha_{2+}\alpha_{3-}(\mu_2+\mu_3)}{C_1g_{m3}\alpha_{3-}}\right)+g_{m2}g_{m3}\alpha_{2+}\alpha_{3-}\right\} \quad (22)$$

The tracking errors and the non-ideal effect of the transconductance of the DDTA can be made negligible by satisfying the following condition:

$$\left.\begin{matrix} \frac{g_{m2}g_{m3}\alpha_{2+}\alpha_{3-}(\mu_2+\mu_3)}{C_1g_{m3}\alpha_{3-}}\ll1 \\ \frac{C_1g_{m3}\mu_3\alpha_{3-}-g_{m2}g_{m3}\alpha_{2+}\alpha_{3-}\mu_2\mu_3}{C_1C_2}\ll1 \end{matrix}\right\} \quad (23)$$

The modified natural frequency (ω_{on}) and the modified quality factor (Q_n) can be expressed as:

$$\omega_{on}=\sqrt{\frac{g_{m2}g_{m3}}{C_1C_2}\cdot\alpha_{2+}\alpha_{3-}} \quad (24)$$

$$Q_n=\sqrt{\frac{C_2g_{m2}}{C_1g_{m3}}\cdot\frac{\alpha_{2+}}{\alpha_{3-}}} \quad (25)$$

To consider the parasitic impedances that affect the proposed mixed-mode filter, the parasitic capacitance C_o and parasitic conductance g_o (g_o=1/R_o, R_o is the output resistance) at the o-terminal of the DDTA are considered while the parasitic impedances at the y- and w-terminals are neglected. Considering Figure 4, the parasitic capacitances C_{o1}, C_{o4} and parasitic conductances g_{o1}, g_{o4} are parallel with C_1 and the parasitic capacitances C_{o2}, C_{o4}, and parasitic conductances g_{o2}, g_{o4} are parallel with C_2. C_{o1}, C_{o2}, C_{o4} are respectively the parasitic capacitances at the o-terminal of $DDTA_1$, $DDTA_2$, $DDTA_4$, and g_{o1}, g_{o2}, g_{o4} are respectively the parasitic conductances at the o-terminal of $DDTA_1$, $DDTA_2$,

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DDTA4. The parasitic capacitances can be neglected by appropriately choosing values such that $C_1 \gg C_{o4} + C_{o4}$, $C_2 \gg C_{o2} + C_{o4}$, $g_{m2} \gg g_{o1}+g_{o4}$, and $g_{m3} \gg g_{o2}+g_{o4}$.

4. Simulation Results

The circuit was designed and simulated using the Cadence Virtuoso System Design Platform using 0.18μm CMOS technology from TSMC. The voltage supply was ±250mV (0.5V) and the bias voltage V_{B1}=-100mV. The transistor aspect ratios are included in Tab. 2.

TABLE II. Transistor aspect ratios of the MIMO-DDTA.

MI-DDA	W/L (μm/ μm)
M_{1A}, M_{2A}, M_{1B}, M_{2B} M_{14}, M_{15}	16/3
M_3-M_8, M_{11}-M_{12}, M_B	8/3
M_9, M_{10}	4/3
M_{16}	6×16/3
M_{13}	6×8/3
M_R	4/5
MIM capacitor: C_B= 0.5 pF, C_c= 6 pF	
MO-TA	W/L (μm/ μm)
M_1, M_2	2×15/1
M_3-M_6, M_{14}-M_{16}	2×10/1
M_{3c}-M_{6c}, M_{14c}-M_{16c}	10/1
M_7-M_{10}, M_{17}-M_{19}, M_{13}	2×15/1
M_{7c}-M_{10c}, M_{17c}-M_{19c}, M_{13c}, M_{11}, M_{12}	15/1

For the filter application, the value of capacitors C_1=C_2=20pF was chosen. The frequency responses of the gain and phase for the differential input VM, non-inverting CM, TAM and TIM filter with I_{set1-4}=4nA are shown in Figure 5. The cutoff frequency was 211 Hz, and the power consumption was 281nW.

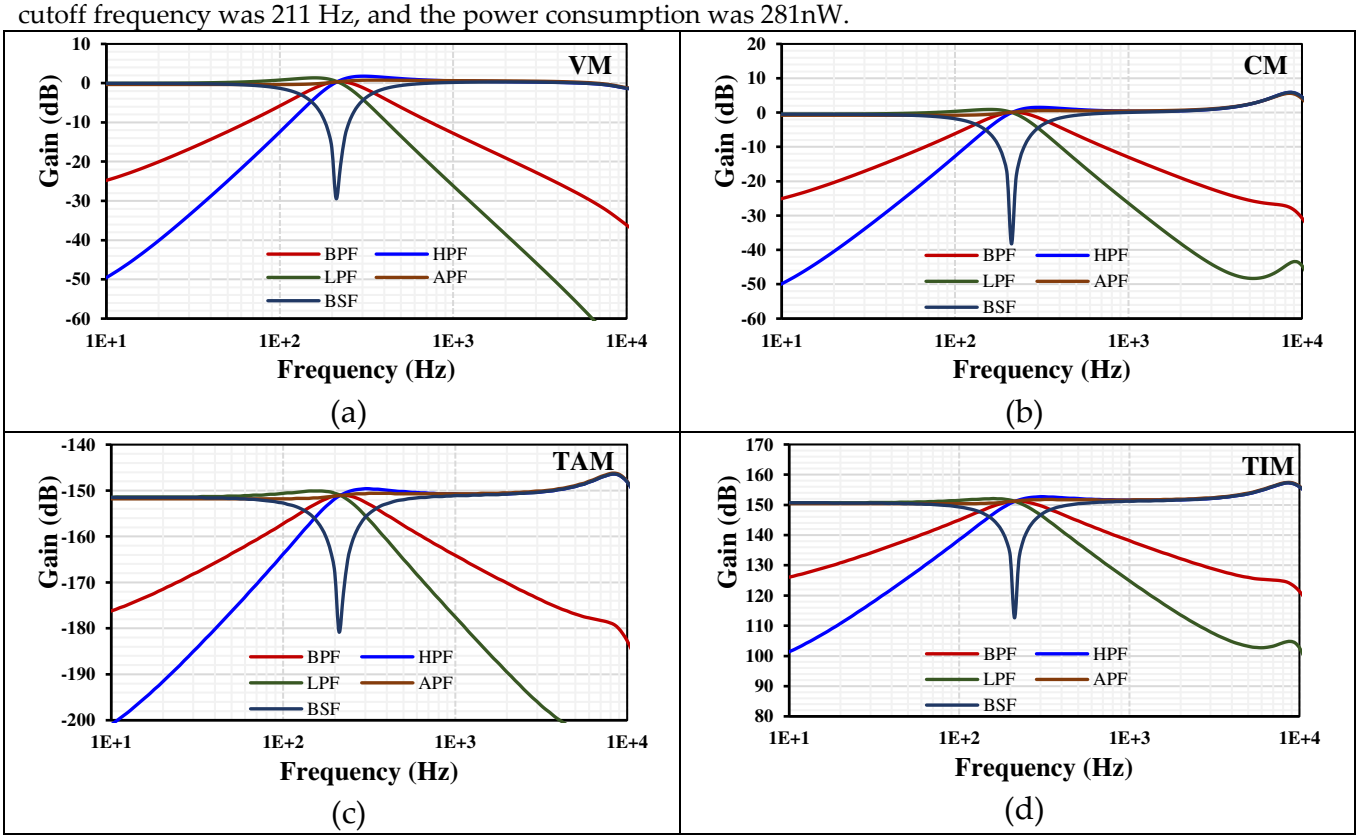

Figure 5. The frequency characteristics of gains for the VM (a), CM (b), TAM (c), and TIM (d).

The frequency responses of LP, HP, BP, BS, and AP gains and phases for VM are shown in Figure 6. The wide tunability of the filter is achieved by varying the setting current I_{set1-4}=(0.5, 1, 2, 4)nA, where the cutoff frequency was (28, 56, 112, 211)Hz, respectively.

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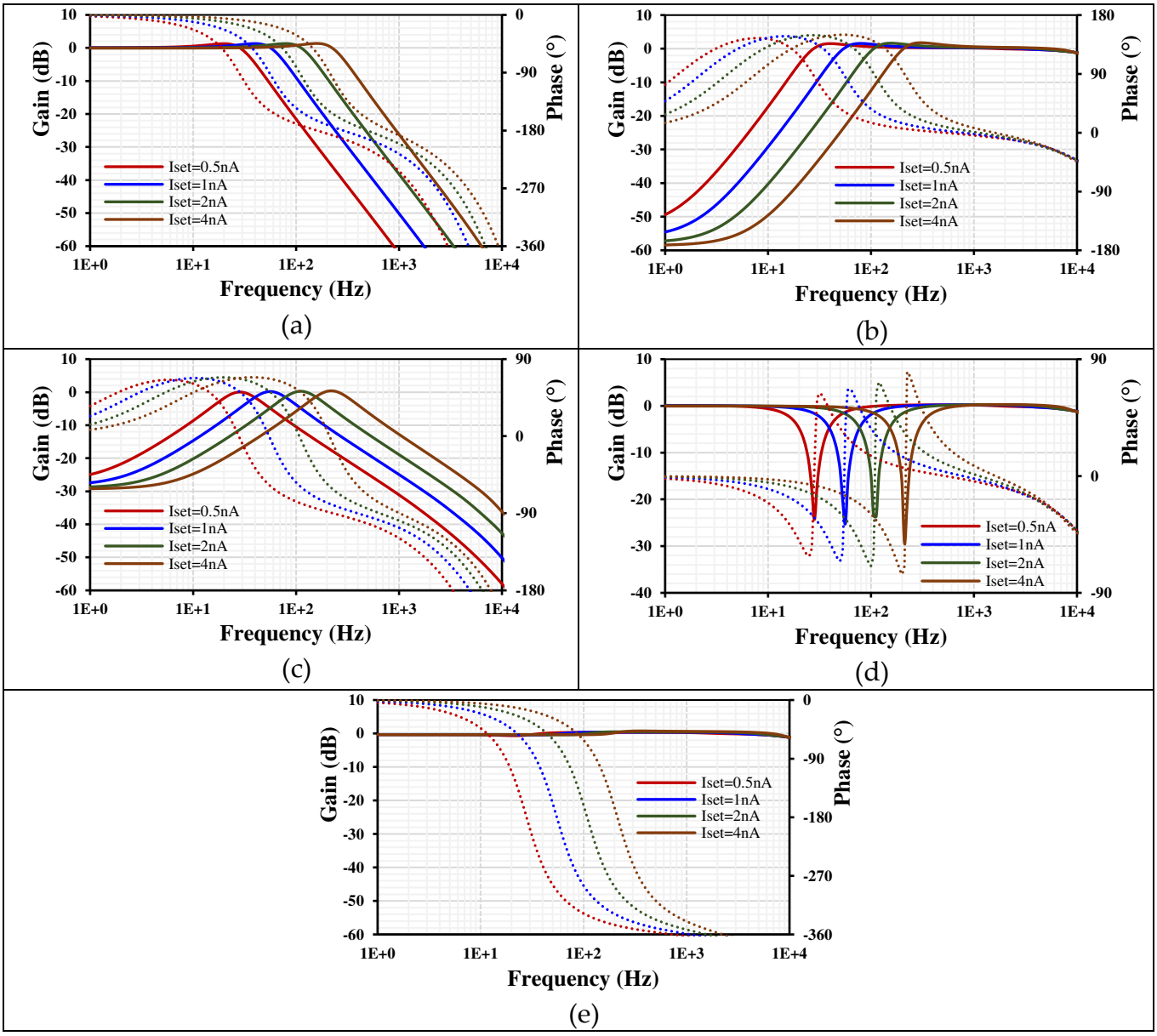
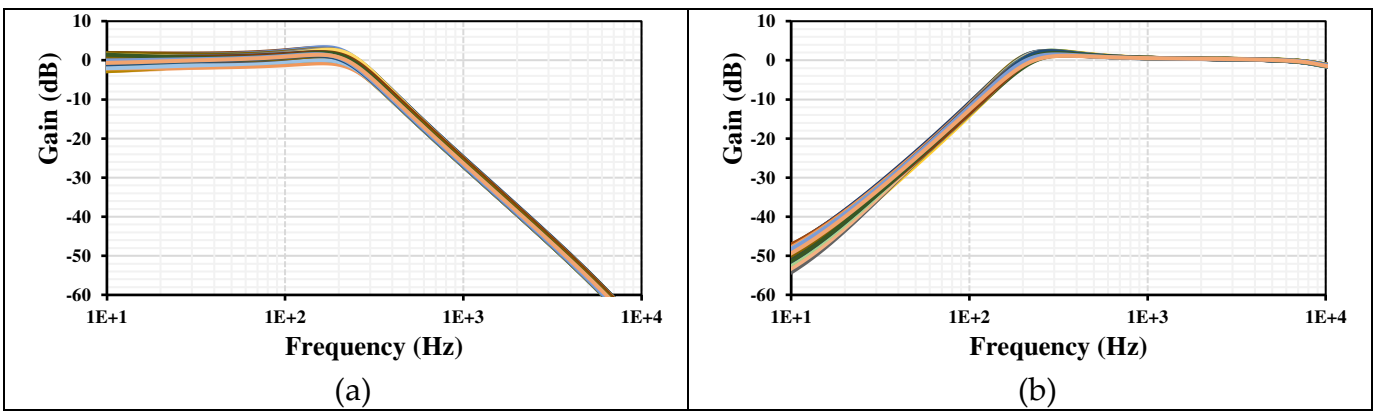


Figure 6. The frequency characteristics of gains (lines) and phases (points) for the VM filter: LPF (a), HPF (b), BPF (c), BSF (d), and APF (e).

Monte Carlo (MC) analysis was used to perform the statistical analysis to estimate the parametric yield and generate information about the performance characteristics of the differential input VM filter. The gains frequency responses of LP, HP, BP, BS, AP with 200 runs MC are shown in Figure 7. The curves are overlapping or close to each other.



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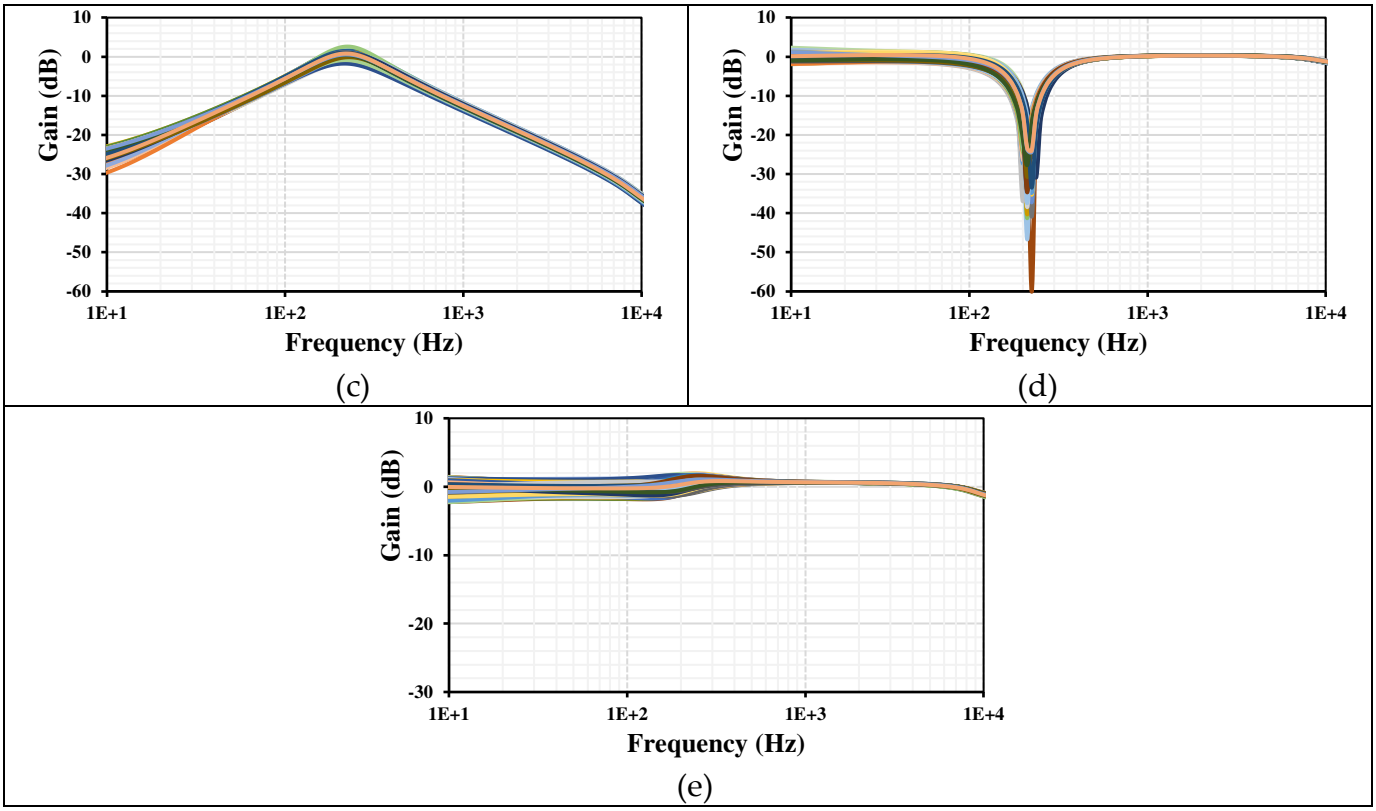
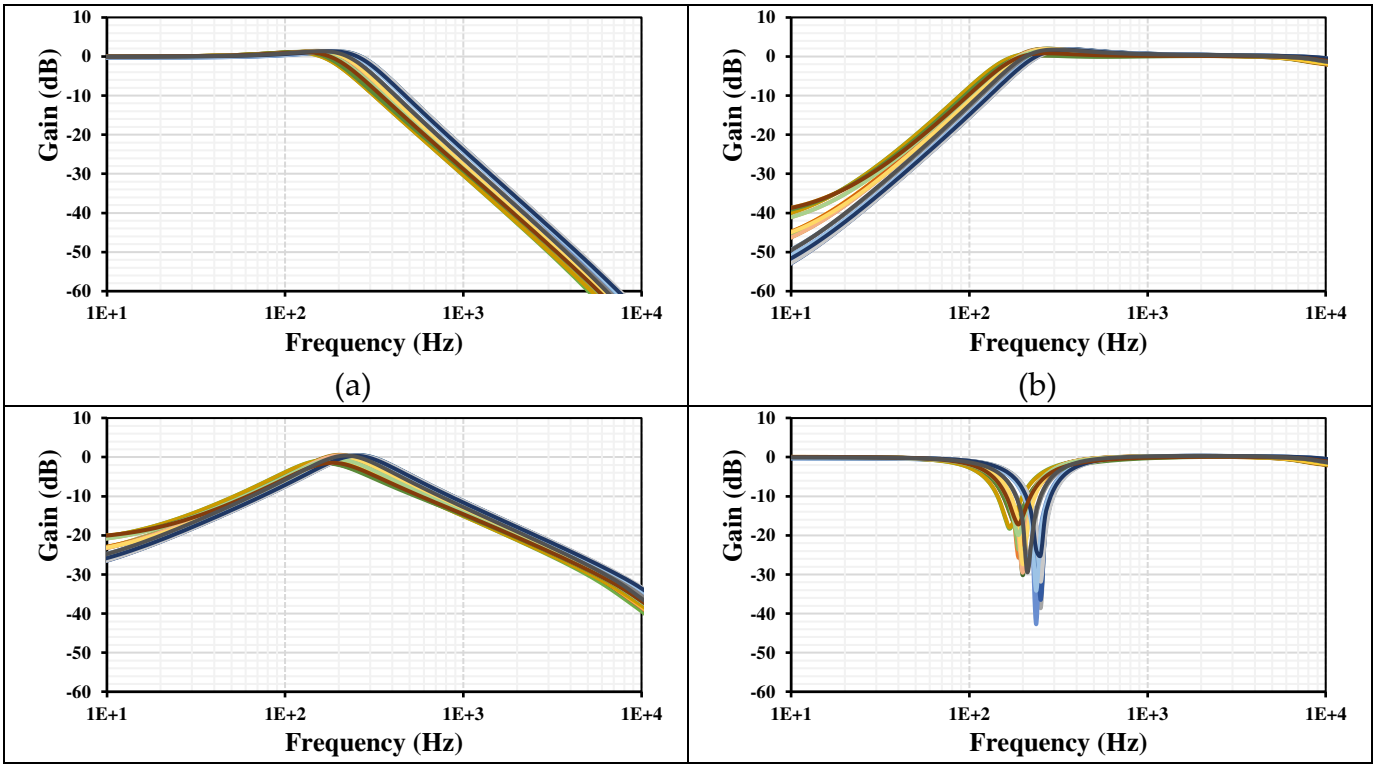


Figure. 7. The 200 runs MC frequency characteristics of the gains for the differential input VM filter: LPF (a), HPF (b), BPF (c), BSF (d), and APF (e).

The process, voltage, temperature (PVT) corners were also used to confirm the robustness of the design. The process transistor corners were: fast-fast, fast-slow, slow-fast, slow-slow. The process MIM capacitor corners were: fast-fast and slow-slow. The voltage supply corners were =±10% (V_{DD}-V_{SS}) and the temperature corners were -20°C and 70°C. The results for the gains frequency responses of LP, HP, BP, BS, AP with PVT are shown in Figure 8. The curves are again overlapping or close to each other, which confirms the robustness of the filter design. Any frequency deviation can be easily adjusted by the setting current.



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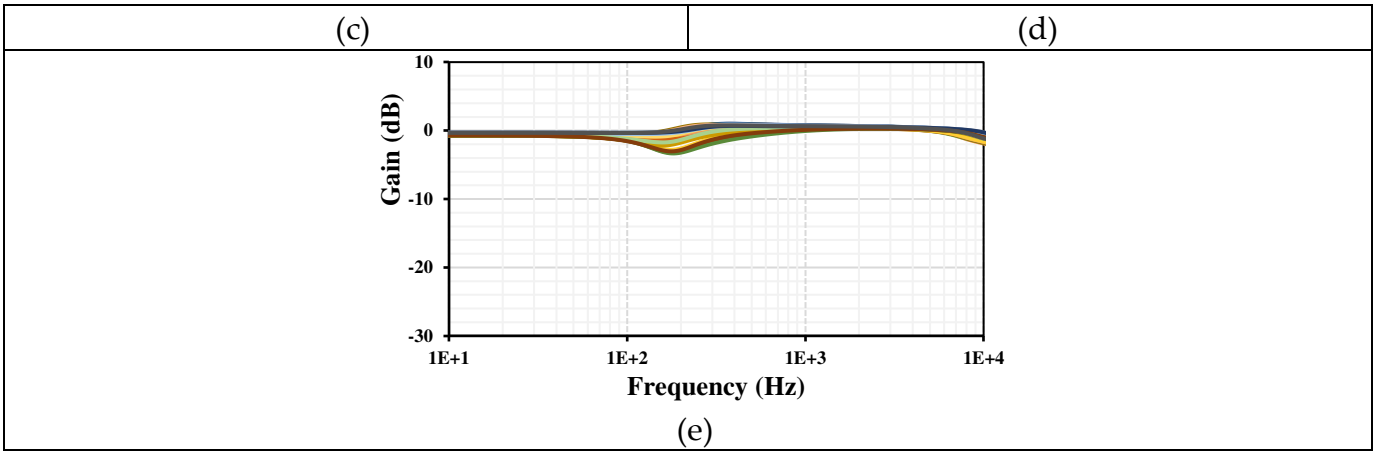

Figure. 8. The PVT frequency characteristics of the gains for the VM filter: LPF (a), HPF (b), BPF (c), BSF (d), and APF (e).

The transient response of the VM LPF with an applied input sinusoidal signal $V_{in\text{-}pp}$=200mV@10Hz is shown in Figure 9 (a). The spectrum of the output signal is shown in Figure 9 (b), where the total harmonic distortion (THD) of 0.23% is indicated.

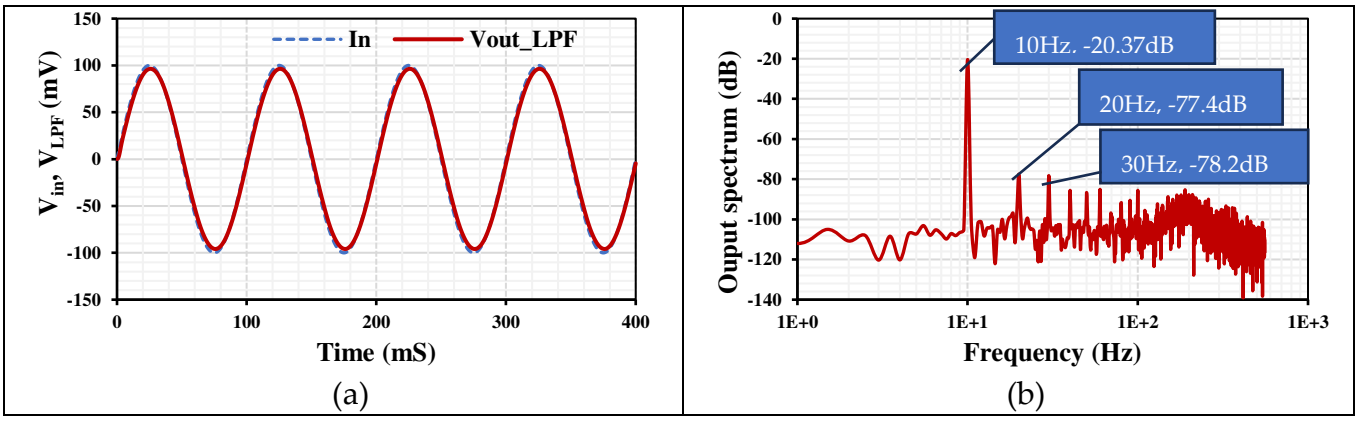

Figure. 9. The transient response of the VM LPF (a) and the spectrum of the output signal (b).

The THD for the VM LPF with different peak-to-peak input signal values @ 10Hz is shown in Figure 10. The 1% THD is achieved for $V_{in\text{-}pp}$=300mV. The output voltage noise for the VM LPF is shown in Figure 11. The root-mean square (RMS) output noise integrated in the bandwidth of 1 to 211 Hz was 130 μV; thus, the dynamic range (DR) of the VM LPF filter is 58.23dB @ 1% THD.

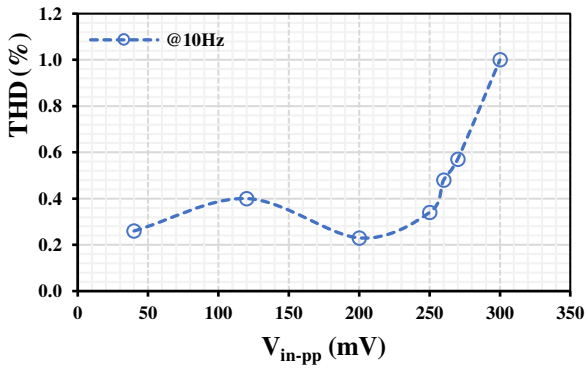

Figure. 10. The THD of the VM LPF with different peak-to-peak input voltages @ 10Hz.

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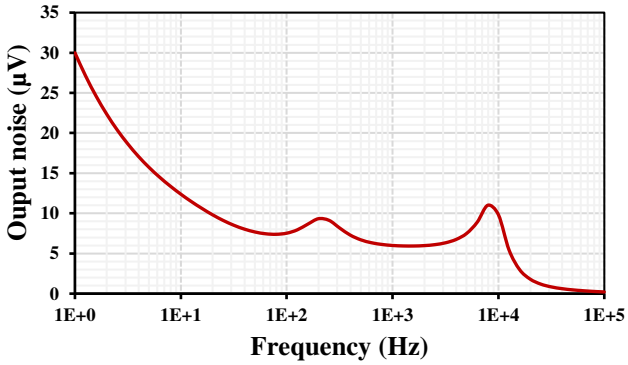

Figure. 11. The output voltage noise of the VM LPF.

The proposed versatile mixed-mode filter was compared with the previously reported filters in [34,37,55,56,65–67] as shown in Table 3. Compared with these previous works, the proposed filter offers the most transfer functions of the five standard filtering functions and the lowest voltage supply. Compared with [34,35], the proposed filter offers electronic tuning capability of the natural frequency; compared with [65–67], the proposed filter uses fewer active devices. The filters in [37,55,56] apply the input signal via capacitor and/or resistor, the structure in [55] does not provide five standard filtering functions of VM, CM, TAM, and TIM, and the filters in [55,56] require input matching conditions for realizing some filtering functions.

TABLE III. Comparison of the proposed filter's properties with those of mixed-mode universal filters.

Factor	**Proposed**	**[34]**	**[37]**	**[55]**	**[56]**	**[65]**	**[66]**	**[67]**
Number of active devices	4-DDTA	3-DDCC	1-FDCCII, 1-DDCC	2-VDBA	3-VDBA	5-OTA	8-OTA	5-DDTA
Realization	0.18 μm CMOS	0.25 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Number of passive devices	2-C	2-C, 3-R	2-C, 6-R	2-C, 2-R	2-C, 1-R	2-C	2-C	2-C
Type of filter	MIMO	MISO	MIMO	MIMO	MIMO	MISO	MIMO	MIMO
Total number of offered responses	61	30	36	17	20	20	20	36
Each mode offers five standard responses	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes
Orthogonal control of ω_o and Q	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Electronic control of ω_o	Yes	No	No	Yes	Yes	Yes	Yes	Yes
All passive devices grounded	Yes	Yes	No	No	No	Yes	Yes	Yes
High input impedances for VM	Yes	Yes	No	No	No	Yes	Yes	Yes
No need for input matching conditions	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes
No need for inverting input conditions	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Power supply (V)	0.5	±1.25	±0.9	±0.75	±1.25	±0.9	±0.3	1.2
Power dissipation (mW)	0.281×10^{-3}	-	-	0.373	5.482	0.1773	0.00577	0.33
Natural frequency (kHz)	0.211	3.315×10^{3}	1.591×10^{3}	1.44×10^{3}	16.32×10^{3}	3.39×10^{3}	5	1.04
Total harmonic distortion (%)	1@300mV_{PP} (LPF)	0.723@60 μA_{PP}	2.2@300 mV_{PP}	2.2@200 mV_{PP}	<4@350m V_{PP} (HPF)	-	2@120mV_{PP} (LPF)	1.09@650 mV_{PP}
Dynamic range (dB)	58.23	-	-	-	-	-	53.2	-

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Verification of result	Sim	Sim	Sim	Sim/Exp	Sim/Exp	Sim	Sim	Sim/Exp

Note: MIMO=multiple-input multiple-output, MISO=multiple-input single-output

5. Conclusions

This paper presents a 0.5-V, 281 nW versatile mixed-mode universal filter using MIMO-DDTAs. The MIMO-DDTA is used to realize a versatile mixed-mode universal filter that offers many transfer functions in the same topology. For the VM LP filter, the dynamic range was 58.23dB @ 1% total harmonic distortion. The proposed filter was designed and simulated in the Cadence Virtuoso System Design Platform using the 0.18μm CMOS technology from TSMC. The simulation results, including Monte-Carlo and PVT corners, confirm the functionality of the design.

Author Contributions: Conceptualization, F. Khateb, M. Kumngern, and T. Kulej; methodology, M. Kumngern and F. Khateb; software, F. Khateb; validation, F. Khateb and T. Kulej; formal analysis, T. Kulej, M. Kumngern, F. Khateb, investigation, F. Khateb and M. Kumngern; resources, F. Khateb, and M. Kumngern; writing—original draft preparation, M. Kumngern, F. Khateb and, T. Kulej; writing—review and editing, F. Khateb, T. Kulej; visualization, F. Khateb, T. Kulej and M. Kumngern; supervision, F. Khateb; project administration, F. Khateb; funding acquisition, F. Khateb and M. Kumngern. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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