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Article

Test structures for the Characterization of the Gate Resistance in 16nm FinFET RF transistors

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Abstract: The gate resistance is a parasitic element in transistors for RF and millimeter-wave circuits that can negatively impact power gain and noise figure. To develop accurate device models, a reliable measurement methodology is crucial. This article reviews the standard measurement methodology used in the literature and proposes also an additional method, which is evaluated using suitable test structures in a 16nm FinFET process. The advantages and disadvantages of the two approaches are discussed along with their respective application scenarios.

Keywords: Gate Resistance, Characterization, de-embedding, radio-frequency MOSFETs (RF MOSFETs), FinFET

1. Introduction

In the last two decades CMOS technologies have become mainstream not only for digital logic but also for RF and millimeter-wave applications. This was possible thanks to the continuous downscaling and layout optimization, which has allowed to reach values of f_t and f_{max} close to 400 GHz [1,2]. The gate resistance R_g is a key parasitic parameter for RF transistors, as it has a significant impact on f_{max} and on the noise performance [3,4]. In order to keep R_g low, circuit designers have to select a suitable geometry for the active devices [5], and to do so it is crucial that the behavior of R_g be correctly captured in the compact models of the transistors. In the last years a lot of research work has been published on this topic, achieving very good results [6–10]. Since the target of any model is to reproduce measurement results as closely as possible, using the best-known measurement methodology is a fundamental pre-requisite. In the reviewed literature the standard common-source structure with open-short de-embedding is always used. In this article we consider also an alternative structure with the transistor connected in capacitor mode, called "capacitor-like" structure, which requires only the open de-embedding step. The article is organized as follows: in section 2 the main features of the two methodologies are presented along with a list of fabricated test structures. In section 3 the capacitor-like structure is analyzed in detail and some design guidelines are derived to achieve accurate measurement results. In section 4 the standard and capacitor-like structures are compared and finally in section 5 the conclusions of this study are presented.

2. Standard and capacitor-like structures - description

The standard method is based on the structure in Fig.1, which consists of an RF transistor in common-source configuration routed to RF GSG pads. This is the structure which is commonly used to extract R_g as well as the other equivalent-circuit parameters of the MOS transistor, and requires open and short structures to de-embed the pads and feedline parasitics. Using the small-signal equivalent circuit of the MOS transistor, the gate resistance can be extracted from the 2-port Y-parameters using the formula $R_g = Re(1/Y_{11})$ [9], under the assumption that the source and drain parasitic resistances R_s and R_d are negligible with respect to R_g.

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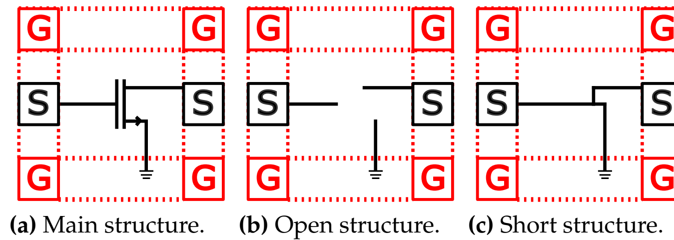
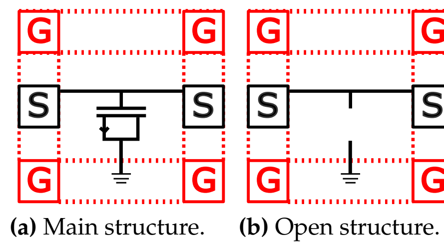
The alternative capacitor-like structure in Fig.2 features the RF transistor connected in capacitor-mode, namely with the gate connected to both input and output pads, and source and drain shorted to ground.



(a) Main structure. **(b)** Open structure. **(c)** Short structure.

Figure 1. Standard structures for Rg measurement.



(a) Main structure. **(b)** Open structure.

Figure 2. Capacitor-like structures for Rg measurement.

One key advantage of this structure is that it requires only the open de-embedding step. Indeed, once we remove the shunt parasitic components of the pads with the open de-embedding, we are left with a T-network formed by the feedlines and the DUT, as shown in Fig. 3. Taking Z_{21} of this network automatically excludes the contribution of the feedlines and no additional de-embedding step is required. Based on considerations very similar to those done for the standard structure, it is found that $R_g = Re(Z_{21})$, again under the assumption that $R_s, R_d \ll R_g$. It should be noted that this concept can not be used in 1-port configuration, as it would require both the open and short de-embedding steps.

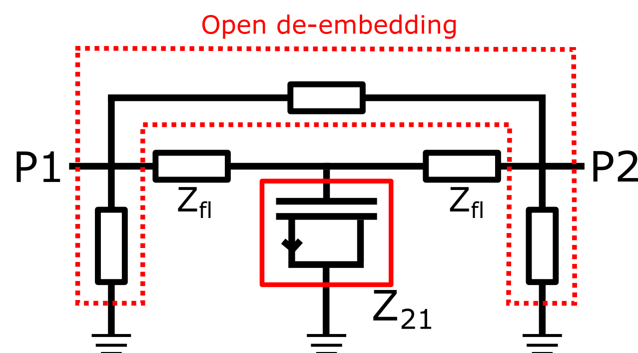


Figure 3. Illustration of the gate resistance extraction methodology using the capacitor-like structure.

For this study 18 test structures utilizing both the standard and capacitor-like concept were fabricated in a 16nm FinFET process. All the structures use nmos RF transistors with the lowest threshold voltage (V_t) and differ in the number of fins (N_{fins}), gate length (L_g) and in the number of devices in parallel, the so-called multiplicity (M). The list of all the available test structures with the related geometrical features is presented in Table 1. In addition to several instances of the capacitor-like structure, three standard structures with different values of M (1,4,8) were fabricated as reference.

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Table 1. List of DUTs on the 16nm FinFET testchip.

DUT	Structure Type	N_{fins}	N_{fing}	L_g[nm]	M
1	Capacitor-like	6	10	20	1
2	Capacitor-like	10	10	20	1
3	Capacitor-like	16	10	20	1
4	Capacitor-like	20	10	20	1
5	Capacitor-like	6	10	20	4
6	Capacitor-like	10	10	20	4
7	Capacitor-like	16	10	20	4
8	Capacitor-like	20	10	20	4
9	Capacitor-like	6	10	20	8
10	Capacitor-like	10	10	20	8
11	Capacitor-like	16	10	20	8
12	Capacitor-like	20	10	20	8
13	Capacitor-like	20	10	16	8
14	Capacitor-like	20	10	18	8
15	Capacitor-like	20	10	24	8
16	Standard	20	10	20	1
17	Standard	20	10	20	4
18	Standard	20	10	20	8

The 2-port S-parameters of the test structures were measured from DC to 110 GHz using a vector network analyzer (VNA) calibrated up to the probe tips. The on-chip interconnections are de-embedded up to the third level of metallization (M3).

In order to assess the quality of the measurement we utilized the relative deviation ΔR_g of the measured gate resistance ($R_{g,meas}$) from the one predicted by the foundry model ($R_{g,sim}$):

$$\Delta R_g = \frac{R_{g,meas} - R_{g,sim}}{R_{g,meas}} \quad (1)$$

It was verified that $R_{g,sim}$ follows the expected scaling law with respect to N_{fins} and M [11], given by:

$$R_g = \frac{R_{conn} + R_{gv}/N_{fins} + R_{gl} \times N_{fins}}{M} \quad (2)$$

where R_{gv} and R_{gl} are respectively the vertical and lateral gate resistance components per fin and R_{conn} is a constant which includes end resistances, contact resistances and interconnects up to M3. This result, shown in Fig.4, justifies the usage of the foundry model as reference to assess the quality of the measured data (eq.1).

3. Capacitor-like structures

This section focuses on the analysis of the capacitor-like structure. The plot of R_g vs frequency in Fig.5 shows very good agreement with the foundry model over the entire frequency range for $V_g = 0.4$ V, whereas the plots of ΔR_g over frequency for different bias conditions in Fig.6 show that the best agreement between measurement and simulation is obtained for $V_g = 0.4$ V. The reason is that the gate resistance consists of a bias-independent contribution from the gate electrode $R_{g,el}$ and a bias-dependent contribution from the channel $R_{ch}(V_g)$ [7,9,12]. In order to predict $R_{g,ch}(V_g)$ accurately, the device section including gate, oxide and channel should be modeled as a distributed RC network [6], which would result in additional complexity of the model and increased simulation time. In order to avoid this, many compact RF models embed the R_{ch} contribution into the bias-independent R_g, assuming for V_g the value which maximizes f_t or f_{max}. This is exactly $V_g = 0.4$ V for this technology and transistor type, which explains why the best agreement between measurement and simulation is attained under this bias condition.

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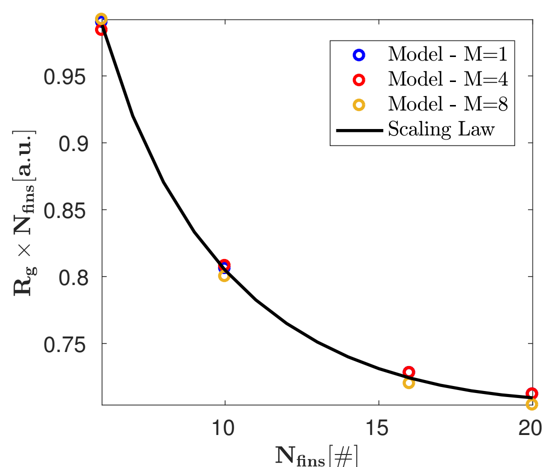

Figure 4. Scaling behavior of gate resistance vs N_{fins} and M obtained from foundry model and from scaling law (eq.2 with $R_{gv} = 155.4\,\Omega$, $R_{gl} = 0.3\,\Omega$, $R_{conn} = 21.7\,\Omega$) with $N_{fing} = 10$, $V_g = 0.4\,$V at $f_0 = 50\,$GHz.

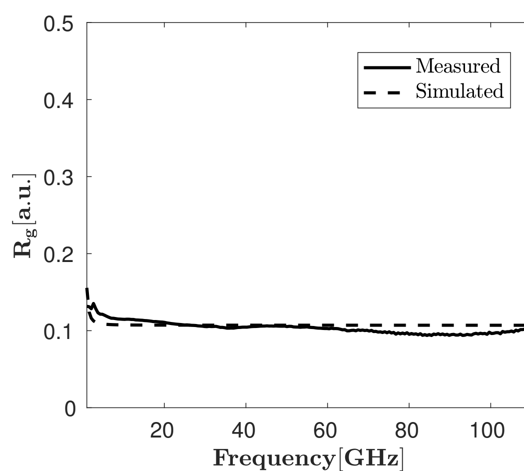

Figure 5. Measured and simulated R_g vs frequency on DUT12 for V_g=0.4 V.

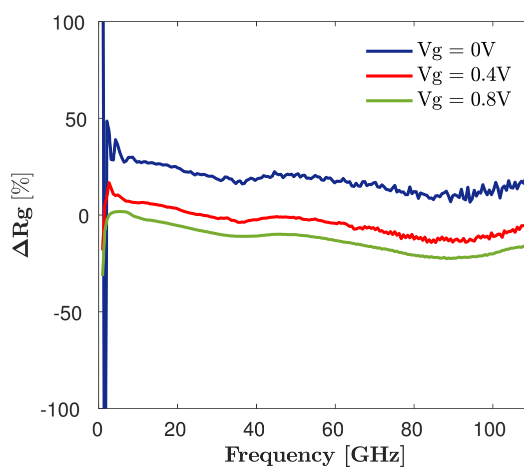

Figure 6. Deviation of the measured gate resistance from simulation on DUT12 for different values of gate bias.

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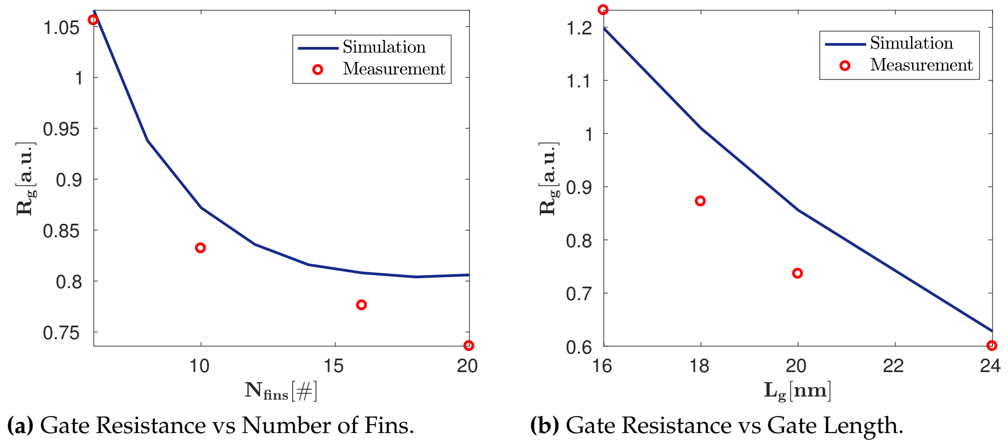
Table 2 reports the values of ΔR_g for different DUTs at $V_g = 0.4\,\text{V}$ and $f_0 = 50\,\text{GHz}$, which is approximately in the middle of the analyzed frequency range. It can be observed that a minimum total device width is required to achieve good agreement between measurement and simulation. The reason is that for the smallest devices like DUT1, the total gate capacitance C_{gg} of the transistor is smaller or comparable to the pad capacitance $C_{pad} \sim 25\,\text{fF}$, which results in a large numerical error in the open de-embedding step. This phenomenon can be also observed simulating the de-embedding process using an approach similar to that of [13]. Based on these considerations, a large value of M should be used if the width of the transistor is small.

Finally, in Fig.7 the measured R_g is compared to simulations as a function of the geometrical parameters N_{fins} and L_g, showing good correlation.

Table 2. ΔRg in % at $f_0 = 50\,\text{GHz}$ with $V_g = 0.4V$ for capacitor-like structures using transistors with various combinations of N_{fins} and M.

M	**N_{fins}**			
	6	**10**	**16**	**20**
1	-52	-18.3	-5.6	3.9
4	9	3.8	4.2	-1.6
8	1.7	-1.8	-4.2	-1.7



(a) Gate Resistance vs Number of Fins.

(b) Gate Resistance vs Gate Length.

Figure 7. Measured and simulated R_g from capacitor-like structures with $M = 4$ at f_0=50 GHz and V_g=0.4 V as a function of N_{fins} and L_g.

4. Comparison between Standard and Capacitor-like structures

In order to make an effective comparison between the two types of structure, standard DUTs 16, 17 and 18 have been included in the teschip, having the same active size as capacitor-like DUTs 4, 8 and 12 respectively. Comparing ΔR_g of the 3 pairs of structures, it is found that the standard structure gives the best results for $M = 1$, as shown in Table 3. Larger values of M (4 and 8) lead to larger deviations and should be avoided. The capacitor-like structure instead is less sensitive on M for the unit device width at hand. All in all, the best achievable ΔR_g with the two structures is comparable.

The second important comparison criterion is the stability of the measured R_g over frequency, which could be potentially influenced by the de-embedding structures. It can be quantified by means of the normalized standard deviation over frequency $\hat{\sigma}_{R_g}/\overline{R_g}$, where $\overline{R_g}$ and $\hat{\sigma}_{R_g}$ are respectively the mean value and the standard deviation of R_g over frequency, defined as:

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Table 3. ΔRg in % at $f_0 = 50\,\text{GHz}$ with $V_g = 0.4V$ for standard and capacitor-like structures with N_{fins}=20, N_{fing}=10, L_g=20 nm and different multiplicities.

Structure Type	M		
	1	4	8
Standard	1.7	16.4	21
Capacitor-like	3.9	-1.6	-1.7

$$\overline{R_g} = \sum_{i=1}^{N} R_g(f_i) \tag{3}$$

$$\hat{\sigma}_{R_g} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(R_g(f_i) - \overline{R_g})^2} \tag{4}$$

with N being the number of frequency points. The normalized standard deviation is plotted in Fig.8 as a function of V_g for the standard and capacitor-like structures with different values of M. It can be observed that the measurements performed with the two structures show similar stability over frequency, with the exception of $M = 8$, for which the capacitor-like structure has lower variance at large V_g values.

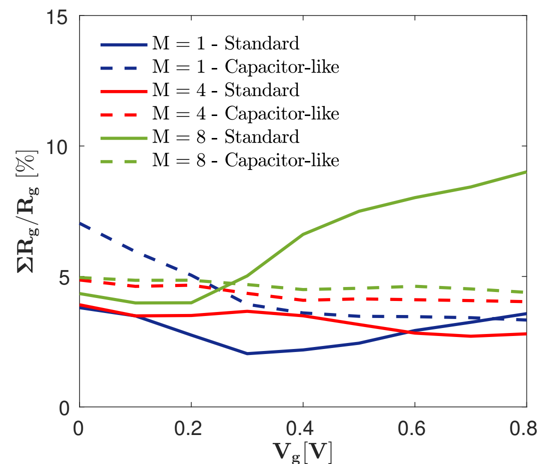

Figure 8. Normalized variance of R_g over frequency as a function of V_g for standard (DUT16,17,18) and capacitor-like (DUT4,8,12) structures.

5. Conclusions

In this article, the standard and capacitor-like structures for the characterization of the gate resistance were analyzed and compared. It was found that the design guidelines to achieve best accuracy in the two types of structure are somehow opposite: for the standard structure there is a constraint on the maximum transistor size, whereas for the capacitor-lilke structure on the minimum size. The two methods show similar accuracy and similar variance over frequency.

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