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Article

Tunneling Current Model under Drain Induced Barrier Lowing Effects for Scaled Devices

Zhichao Zhao, Tiefeng Wu *,Miao Wang, Yunfang Xi, Qiuxia Feng and Yonghao Sun

School of Information and Control Engineering, Qingdao University of Technology, Qingdao 266520
* Correspondence: wutiefeng@qut.edu.cn; Tel.:86-18745452655

Abstract: With the proportional reduction of MOSFET size, the leakage-to-barrier reduction (DIBL) effect leads to a more significant increase in the tunneling current on the gate, and the appearance of the gate tunneling current also seriously affects the static characteristics of the device. In this paper, a new theoretical model of the relationship between the direct tunneling current and the thickness of the oxide layer under the DIBL effect is proposed for the MOSFET device with ultra-thin oxide layer. On this basis, the characteristics of the MOSFET device are studied in detail by using HSPICE, and their working conditions are quantitatively analyzed. The characteristic variation trend of small-size devices under the influence of gate tunneling current is predicted. The simulation results using BSIM4 model are consistent with the theoretical model. The theory and data in this paper will provide useful reference for large scale integrated circuit design.

Keywords: scaled device; ultra-thin gate oxide; DIBL; direct tunneling current

1. Introduction

Si materials dominate the semiconductor devices and integrated circuits. For scaled MOSFET devices, with thinner thickness of the gate oxide layer, the effect of gate tunneling current on the performance of the device is more significant. With DIBL effects, the direct tunneling current of MOSFET devices will also change significantly. With thinner thickness of the gate oxide layer, gate tunneling current of MOSFET will become larger, and gate tunneling current is the major component of MOSFET off-state leakage currents [1]. According to the existing domestic and foreign literature, tunneling current has been widely modeled, however, these studies did not consider the DIBL effect. And these models are also not suitable for predicting the characteristics and tunneling current trends of MOSFET devices with thinner oxide layers [2-5].

Herein, to illustrate the relationship between gate oxide film thickness and gate direct tunneling current of MOSFET devices, a gate tunneling current model with DIBL effect is presented in this paper. As shown in Figure 1, in this model, the tunneling current of overlapping dimension and gate is studied as a group, and the influence of direct tunneling current under the DIBL effect on the off-state characteristics of MOSFET devices is carefully studied. In the paper, the off-state characteristics of MOSFET devices are simulated, the static characteristics include the relations between leakage current and gate oxide film thickness in 0.7~1.3nm. The trend of gate tunneling current of scaled MOSFET devices is determined. When the oxide film thickness of devices decreases proportionally, the corresponding device parameters will also change, so the effects of other parameters such as doping concentration are also taken into account in the simulation [6-8]. Through comparison simulation results and theoretical result, this model is proved to be highly reliable. This provides a useful theoretical basis for future circuit design, which is helpful for circuit design of small size devices.

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2. Tunneling Current Model

2.1. DIBL Effects

Drain Induced Barrier Lowering (DIBL) effect is a very important physical phenomena in scaled devices. As channel length becomes shorter, threshold voltage is more dependent on channel length and drain bias. Threshold voltage dependence on the body bias becomes weaker control of the depletion region. Because of threshold voltage reduction caused by drain voltage, DIBL effect becomes an important physical limitation for device applications [9]. Especially in sub-threshold case, the enhancement of carrier injection at the source leads to an increases of sub-threshold leakage current. It is necessary to calculate exactly leakage current by building tunneling current model with DIBL effect.

In DIBL effects, the threshold voltage $V_{TH.D}$ can be described by formulation (1), ΔV_{TH} is threshold voltage increment in equation (1) and (2) [10].

$$V_{TH.D} = V_{TH} + \Delta V_{TH}, \quad (1)$$

$$\Delta V_{TH} = \frac{-0.5}{\cosh(K \cdot \frac{L_{eff}}{l_{t0}}) - 1}(m_1 + m_2 \cdot V_{BS}) \cdot V_{DS}, \quad (2)$$

In formulation (2), L_{eff} is effective length, l_{t0} and X_{dep0} can be obtained from formulations (3) and (4), K is the constant of gate insulator (value 3.9), m_1, m_2 are technological parameters obtained by parameter extraction, X_{dep0} is depletion edge when $V_{BS} = 0$, n_d is channel doping density of zero-bias (value 1.7e17cm^{-3}), n_i is channel carrier density, ε_{Si} is dielectric coefficient of silicon, ϕ_s is surface voltage, T_{ox} is thickness of gate oxide layer.

$$l_{t0} = \sqrt{\frac{\varepsilon_{Si} T_{ox} X_{dep0}}{K}}, \quad (3)$$

$$X_{dep0} = \sqrt{\frac{2\varepsilon_{Si}\phi_s}{q n_d}}, \quad (4)$$

Surface potential can be express as equation (5), k is Boltzmann constant, q is charge quantity, T is absolute temperature, $PHIN$ shows in equation (6).

$$\phi_s = 0.4 + \frac{kT}{q}\ln(\frac{n_d}{n_i}) + PHIN, \quad (5)$$

$$PHIN = -qD / \varepsilon_{Si}, \quad (6)$$

Since $\phi_s = \varphi_s + V_{BS}$, the value of potential φ_s is $\phi_s = \varphi_s$, so equation (7) can be obtained.

$$\varphi_s = 0.4 + \frac{kT}{q}\ln(\frac{n_d}{n_i}), \quad (7)$$

2.2. Gate Direct Tunnel Current Model

As shown in Figure 1, the gate direct tunnel current consists of four parts, I_{gb} is gate-to-substate leakage current, I_{gso} and I_{gdo} are parasitic leakage current through the gate-to-source-drain overlap area, I_g is gate-to-inversion channel tunnel current, I_{gc} flows to source (I_{gcs}), and I_{gcd} flows to drain.

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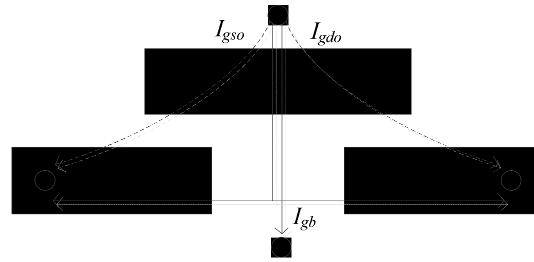

Figure 1. Composition of gate tunneling current.

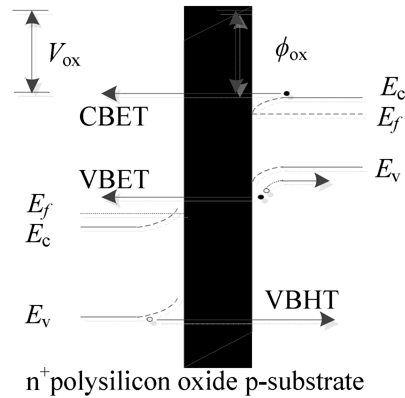

Figure 2. Tunneling Current Physical Mechanism.

Gate direct tunneling current is generated by tunneling electrons or holes reaching gate through the gate oxide barrier. The direct tunneling is shown in Fig. 2. ϕ_{ox} is height of oxide barrier, V_{ox} is the potential difference of the gate oxide, E_f is Fermi energy level, E_c is conduction band, E_v is valence band, A and B are physical constants that depend on ϕ_{ox} and the effective mass of tunneling particle. In this paper, the characteristics of the gate tunneling current as a group in the off state are mainly studied, especially the relationship between gate tunneling current and the thickness of the oxide layer. The relation model between gate direct tunneling current and gate oxide thickness is deduced. The gate direct tunneling current of MOSFET devices [11,12] can be modeled as

$$J_{DT} = J_G = AE_{ox}^2 \cdot \exp[-BE_{ox}^{-1}(1-(1-\frac{V_{ox}}{\phi_{ox}})^{\frac{3}{2}})], \tag{8}$$

When $1-(1-\frac{V_{ox}}{\phi_{ox}})^{\frac{3}{2}} \approx 1$, the gate tunneling current along x point will be approximately

$$\begin{aligned} J_G(x) &\approx AE_{ox}^2 e^{-B/E_{ox}} \\ &\approx AE_{oxs}^2 e^{-BT_{ox}/(V_{oxs}-V(x))}, \\ &\equiv J_{G0} e^{-B^* V(x)} \end{aligned} \tag{9}$$

In equation (9), J_{G0} is gate tunneling current density ($V_{DS} = 0$), $B^* = pBT_{ox}/V_{oxs}^2$, T_{ox} is the thickness of oxide layer, p is a tuning parameter with default 1, $V_{oxs} \approx V_{GS}$, is the gate-source voltage at $x = 0$. If the gate leakage current is much less than the drain current, then

$$V(x)=V_{GS}-V_{TH.D}-\sqrt{(V_{GS}-V_{TH.D})^2-2(V_{GS}-V_{TH.D}-V_{DS}/2)V_{DS}\cdot x/L} \approx (V_{GS}-V_{TH.D}-V_{DS}/2)\cdot V_{DS}/(V_{GS}-V_{TH.D})L\cdot x, \quad (10)$$

Accurate tunneling current model is shown in equation (11). Its physical meaning is that total amperage is equal to the product of gate-oxide interface area (WL) and average current density $<J_G(x)>$ across the interface, $J_{G(x)}=J_{G0}e^{-B^*V(x)}$ is gate tunneling current density at x. By equations (2), (3) and (4), might as well assume $-B^*k=p$, $k=(V_{GS}-V_{TH.D}-V_{DS}/2)\cdot V_{DS}/(V_{GS}-V_{TH.D})L$, the total gate tunneling current can be obtained by equation (12).

$$I_G=W\int_0^L J_G(x)dx=(WL)\cdot\frac{\int_0^L J_G(x)dx}{\int_0^L dx}=(WL)\cdot<J_G(x)>, \quad (11)$$

$$\begin{aligned}I_G&=W\int_0^L J_{G0}e^{px}dx=J_{G0}W\frac{1}{p}(e^{pL}-1)=\frac{J_{G0}W}{p}e^{pL}-\frac{J_{G0}W}{p}\\&=\frac{J_{G0}WL(V_{TH.D}-V_{GS})}{B^*[(V_{GS}-V_{TH.D})V_{DS}-V_{DS}^2/2]}\exp\left(\frac{-B^*V_{DS}(V_{GS}-V_{TH.D}-V_{DS}/2)}{V_{GS}-V_{TH.D}}\right),\\&+\frac{J_{G0}WL(V_{GS}-V_{TH.D})}{B^*[(V_{GS}-V_{TH.D})V_{DS}-V_{DS}^2/2]}\end{aligned} \quad (12)$$

It can be simplified to

$$I_G=\frac{J_{G0}WL(V_{TH.D}-V_{GS})}{B^*[(V_{GS}-V_{TH.D})V_{DS}-V_{DS}^2/2]}e^{-B^*/C}+J_{G0}WLC/B^*, \quad (13)$$

When substrate bias V_{BS}=0,

$$\Delta V_{TH}=\frac{-0.5m_1V_{DS}}{\cosh(m_3\frac{L_{eff}}{l_{t0}})-1}=-\frac{1}{2}m_1V_{DS}\frac{1}{\cosh\left(\frac{m_3L_{eff}}{\sqrt{\frac{\varepsilon_{Si}T_{ox}X_{dep0}}{K}}}\right)-1}, \quad (14)$$

m_3 is process parameters obtained by parameter extraction, since $cosh=(e^x+e^{-x})/2$, so

$$\Delta V_{TH}=\frac{V_{DS}m_1}{1-e^{\sqrt{T_{ox}}}\left(e^{\frac{m_3L_{eff}}{\sqrt{\frac{\varepsilon_{Si}T_{ox}X_{dep0}}{K}}}}+e^{\frac{-m_3L_{eff}}{\sqrt{\frac{\varepsilon_{Si}T_{ox}X_{dep0}}{K}}}}\right)}=\frac{V_{DS}m_1}{1-K_1e^{\sqrt{T_{ox}}}}, \quad (15)$$

Let K_1 denote the hyperbolic function in equation (15), the direct tunneling current model (Eq.19) of scaled down devices under the DIBL effects can be obtained by equations (17) and (18).

$$K_1=e^{\frac{m_3L_{eff}}{\sqrt{\frac{\varepsilon_{Si}T_{ox}X_{dep0}}{K}}}}+e^{\frac{-m_3L_{eff}}{\sqrt{\frac{\varepsilon_{Si}T_{ox}X_{dep0}}{K}}}}, \quad (16)$$

$$\frac{C}{B^*}=\frac{1}{T_{ox}}\frac{V_{GS}^2}{pB}\frac{V_{GS}-V_{TH}-\frac{V_{DS}m_1}{1-K_1e^{\sqrt{T_{ox}}}}}{(V_{GS}-V_{TH}-\frac{V_{DS}m_1}{1-K_1e^{\sqrt{T_{ox}}}})V_{DS}-\frac{1}{2}V_{DS}^2}, \tag{17}$$

$$\frac{-B^*}{C}=T_{ox}\cdot\frac{pBV_{DS}}{V_{GS}^2}(1-\frac{1}{2}\frac{V_{DS}}{V_{TH}+\Delta V_{TH}-V_{GS}})\overset{K_2=\frac{pBV_{DS}}{V_{GS}^2}}{=}T_{ox}\cdot K_2(1-\frac{1}{2}\frac{V_{DS}}{V_{TH}+\Delta V_{TH}-V_{GS}}), \tag{18}$$

$$I_G=J_{G0}WL\frac{C}{B^*}(1-e^{-B^*/C})$$
$$=J_{G0}WL\frac{1}{T_{ox}}\frac{V_{GS}^2}{pB}\frac{V_{GS}-V_{TH}-\frac{V_{DS}m_1}{1-K_1e^{\sqrt{T_{ox}}}}}{(V_{GS}-V_{TH}-\frac{V_{DS}m_1}{1-K_1e^{\sqrt{T_{ox}}}})V_{DS}-\frac{1}{2}V_{DS}^2}[1-\exp(T_{ox}K_2(1-\frac{\frac{1}{2}V_{DS}}{V_{TH}-V_{GS}+\frac{V_{DS}m_1}{1-K_1e^{\sqrt{T_{ox}}}}}))] \tag{19}$$

3. Static Characteristics Simulation

In simulation, the BSIM4 model is particularly important due to its wide application in industry, so all the analysis in this paper use BSIM4 model[13], and simulation tool is HSPICE. The device structure parameters and their values show in Table 1 when simulating static gate tunneling current of NMOSFET.

When studying the characteristics of MOSFET devices, dielectric oxide is SiO_2. There are two main reasons. Firstly, the circuit performance is limited by operating voltage, noise margin and power, so Relevant characteristics need to be determined quantitatively. Secondly, the simulation framework can use in the devices whose oxide layer composed by the other dielectric, and it can evaluate the performance between SiO_2 dielectric and the other dielectric.

Based on the BSIM4 model and different bias states, using HSPICE, the variations of gate direct currents for MOSFET were simulated. Structure parameters of device were shown in Table 1, and the device simulation results were shown in figures 3~8. Figure 3 and 4 show the simulation results at two cut-off states for NMOSFET. The NMOSFET is biased in two cut-off states respectively, $V_{GS.N}=0, V_{DS.N}=0{\sim}V_{DD}$ and $V_{DS.N}=0, V_{GS.N}=0{\sim}V_{DD}$. Figure 5 and 6 show the simulation results at two cut-off states for PMOSFET similar to NMOSFET. It can be seen from the figures when the normalized drain-source voltage is changed from 0 to 1.0V, the gate tunneling current of the technology node with gate length of 90~65nm remains almost unchanged, while the gate tunneling current of the technology node with gate length of 53~40nm increases significantly and rapidly. It can be found that the thinner the thickness of gate oxide layer, the faster of gate direct tunneling current increases. When the thickness of gate oxide layer decreases from 1.3nm to 0.7nm, the gate tunneling current increases by about three orders of magnitude, namely, from 10^{-9}(A) to 10^{-6}(A). In Figure 7, considering DIBL effect, the NMOSFET is biased in the off state $V_{GS}=0, V_{DS}=0{\sim}V_{DD}$. It can be found that the gate tunneling current is greater than without DIBL effect.

Figures 3~7 show the increase of gate tunneling current when the gate oxide layer thickness decreases, and this increasing function can be obtained. To further illustrate the growth of gate tunneling current function, it will be explained by figure 8. Solid line shows theoretical exponential curve at $V_{TH.D}=V_{TH}$ obtained by model (13), and dotted line represents theoretical curves obtained from model (19) and increases exponentially. The simulation results and theoretical results are given by figure 8. The simulation and theory

research show the same results. It can fully prove the rationality and effectiveness of Model (19) proposed in this paper.

Table 1. Structure Parameters of Device.

Name	Parameters	Values					
Gate length	L_{min} (nm)	90	75	65	53	45	40
Channel length	L_{ch} (nm)	65	53	45	37	32	28
Overlap dimension length	$L_{g.ov}$ (nm)	12.5	11.0	10.0	8.0	6.5	6.0
Oxide layer thickness	T_{ox} (nm)	1.3	1.2	1.1	0.9	0.8	0.7
Supply voltage	V_{DD} (V)	1.2	1.1	1.0	1.0	0.9	0.9
Threshold voltage	V_{TH} (V)	0.35	0.33	0.32	0.30	0.28	0.27
Junction depth	X_j (nm)	71.5	58.5	49.5	36.0	35.5	31.5
Substrate dopant concentration	N_{sub} ($10^{19}cm^{-3}$)	0.4	0.6	0.8	1.1	1.4	1.6
Transition depth	X_{tr} (nm)	35	29	25	18	18	16
Channel dopant concentration	N_{ch} ($10^{18}cm^{-3}$)	1.15	1.15	2.0	2.0	2.0	3.0
Gate dopant concentration	N_{gate} ($10^{20}cm^{-3}$)	0.92	0.92	1.14	1.5	1.66	1.66

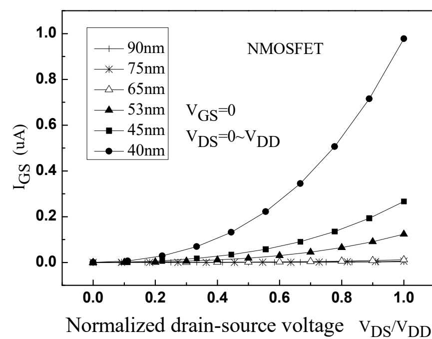

Figure. 3 Gate Current V_{GS}=0 for NMOSFET

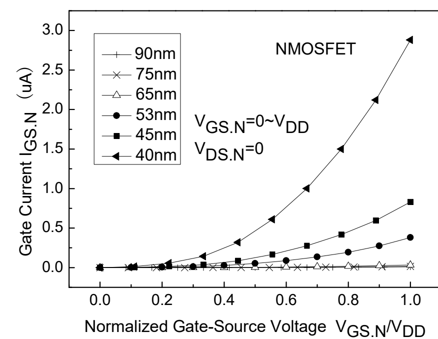

Figure. 4 Gate Current V_{DS}=0 for NMOSFET

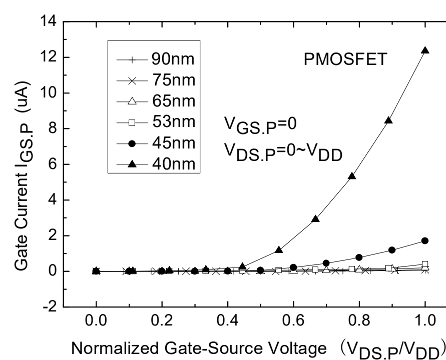

Figure. 5 Gate Current V_{GS}=0 for PMOSFET

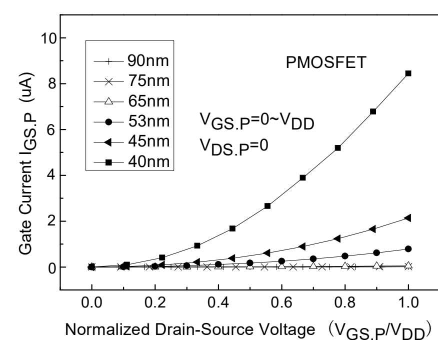

Figure. 6 Gate Current V_{DS}=0 for PMOSFET

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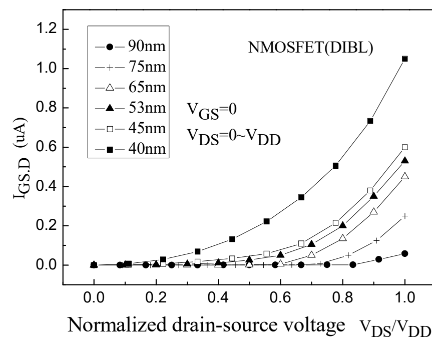

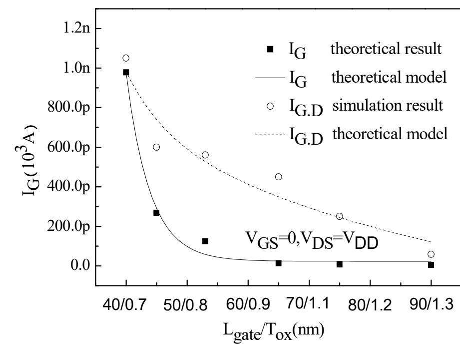

Figure. 7 Gate Current under DIBl Effect V_{GS}=0 **Figure. 8** Comparing of Tunneling Current trends

4. Discussion

Based on the physical mechanism of tunneling current, the theoretical model of gate tunneling current is derived with DIBL effect. It mainly indicates that the thickness of the gate oxide layer decreases proportionally, the gate tunneling current increases exponentially. Based on BSIM4 model, using HSPICE, the simulation results can be obtained. In different off states, quantitative study is made on gate tunneling current using silica as insulator. For MOSFET devices, the simulation results consistent with the theory model derived. In addition, the simulation framework used in this paper can not only provide theoretical and experimental basis for future circuit design, but also can be used to evaluate the performance differences when other dielectrics are used as insulating layers.

Supplementary Materials: Figure S1: title; Table S1: title; Video S1: title.

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