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Article

Research and Comparative Modeling of the Si, GaAs and GaN JFET/CMOS Buffer Amplifiers for Sallen-Key LPF Design Problems with A Low Offset Voltage's Systematic Component

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Abstract: The authors of the article performed computer simulation of buffer amplifiers (BA), which have medium and extremely small values of the offset voltage's systematic component (V_{off}), for different technological processes (Si, GaAs and GaN). The proposed control units are distinguished by a small number of elements and allow operation in the range of low and high temperatures. The variants of circuitry implementation of control units based on GaAs, GaN depletion-mode CMOS and JFET technological processes are considered. The results of the comparative modeling showed that the basic circuit of the BA on two field-effect transistors, when implemented on various modifications of GaN MOS and depletion-mode MOS transistors, provides sufficiently low values of the offset voltage's systematic component (less than 2 μV). The proposed BAs are designed for use in the structure of the Sallen-Key low-pass filter (LPF) when they are implemented both on mid-frequency Si CJFET and on GaAs microwave transistors. Low values of the LPF V_{off} have a positive effect on the effective capacity of the ADC. An example of switching on a BA in the JFET OpAmp structure based on the depletion-mode MOS input stage and a "folded" cascode, which, with 100% negative feedback, can be used in the Sallen-Key LPF, is considered. Computer simulation of the JFET/MOS OpAmp showed that the OpAmp has an open-loop voltage gain of 76-85dB, and its V_{off} is within 7μV in the temperature range from -60°C to +120°C. The presented circuitry of buffer amplifiers is intended, first of all, for the tasks of designing precision Sallen-Key low-pass filter (low-pass filter, high-pass filter, PF, RF).

Keywords: analog circuit design; buffer amplifiers; offset voltage's systematic component; voltage followers; operational amplifiers; depletion-mode; CMOS; JFET; Si; GaAs; GaN

1. Introduction

Buffer amplifiers (BAs), as well as voltage followers on operational amplifiers (OpAmps) with 100% negative feedback, which have a voltage transfer coefficient close to unity, are quite an important functional unit of many analog devices [1-5]. Promising control units based on field-effect transistors with a control p-n-junction (JFET), as well as field-effect CMOS (in enhancement-mode and depletion-mode) transistors [6]. Two-transistor BA circuit solutions can be popular in Sallen-Key anti-aliasing low-pass filters, switched on at the ADC input to limit the spectra of input signals.

The main goal and novelty of the article is a comparative computer simulation of basic buffer amplifier circuits for Si, GaAs, GaN depletion-mode CMOS and JFET technological processes with reduced static currents, as well as low and ultra-low values of the offset voltage's systematic component.

2. CJFET BA with adjustable level of the offset voltage's systematic component

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In the low-temperature CJFET buffer amplifier circuit in Fig.1 [7] the static current mode of field-effect transistors M1 and M2 is determined by one current-stabilizing resistor R1.

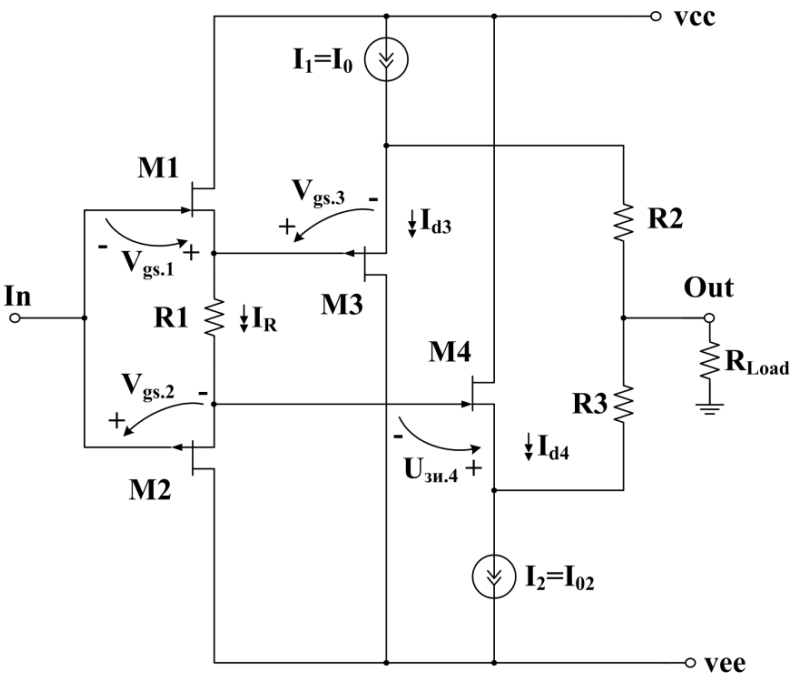

Figure 1. CJFET BA with low offset voltage's systematic component.

This allows, by changing its resistance, to select the specified values of the drain currents (I_{d1}, I_{d2}) of these active elements:

$$I_R = I_{d1} = I_{d2} = \frac{V_{gs.1} + V_{gs.2}}{R_1}$$

where $V_{gs.i}$ is the gate-source voltage of the *i*-th field-effect transistor at a source current equal to I_R.

By optimizing the numerical values of the resistances R2 and R3 in the circuit, a low level of the offset voltage's systematic component is provided. In this case, the resistances R2, R3 can range from hundreds of Ohms to ten kOhms. In addition, adjusting the parameters of the reference current sources I_1 and I_2, as well as the number of transistors connected in parallel (for example, NM3=NM4=3 pcs.) or the width of their channels to obtain small V_{off} in the CJFET BA circuit in Fig. 2.1 can be implemented. As a result of optimization and computer simulation of the buffer amplifier (Fig.1) in the LTSpice environment at room temperature, as well as at cryogenic temperatures, a low offset voltage's systematic component was obtained (at the level of tens of microvolts, without taking into account the technological spread of element parameters) (Fig. 2a). The amplitude-frequency characteristic (AFC) of the BA for different temperatures is shown in Fig. 2b with resistors R1=100kOhm and R2=7.9kOhm, R3=7.79kOhm.

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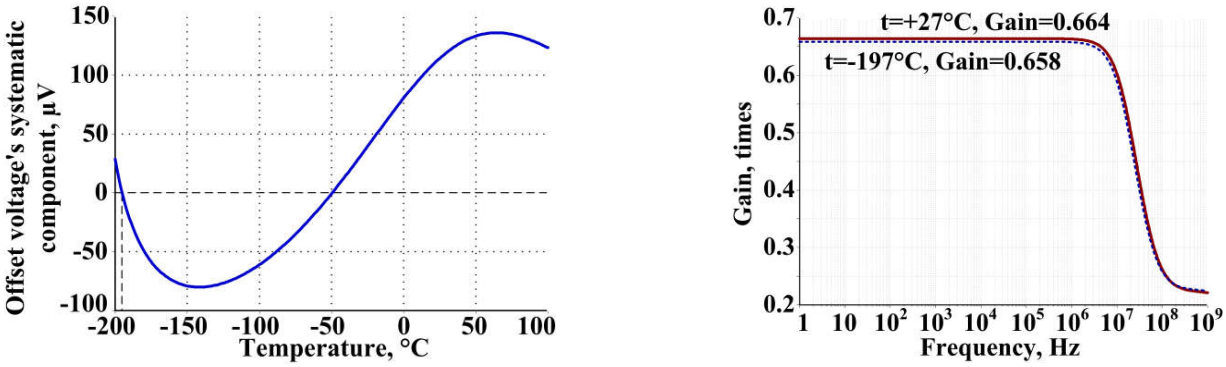

Figure 2. The dependence of the offset voltage's systematic component (a) and the AFC of the gain (b) of the optimized CJFET BA circuit in Fig. 2.1 at t=-197°C.

Computer simulation of the BA (Fig. 2.2) [7] in the LTSpice environment shows that its static current consumption is measured in tens of microamperes (I_{cons} = 47 µA), and this circuit is adapted for use in the low temperature range (up to -197ºC).

3. Buffer amplifiers with extremely low offset voltage's systematic component

In the developed buffer amplifier circuit in Fig. 3, the static current mode of the field-effect transistors M1 and M2 is determined by the current-stabilizing resistors R1 and R2, which makes it possible, by changing their resistances, to select the specified drain current values (I_{d1}, I_{d2}) of these active elements.

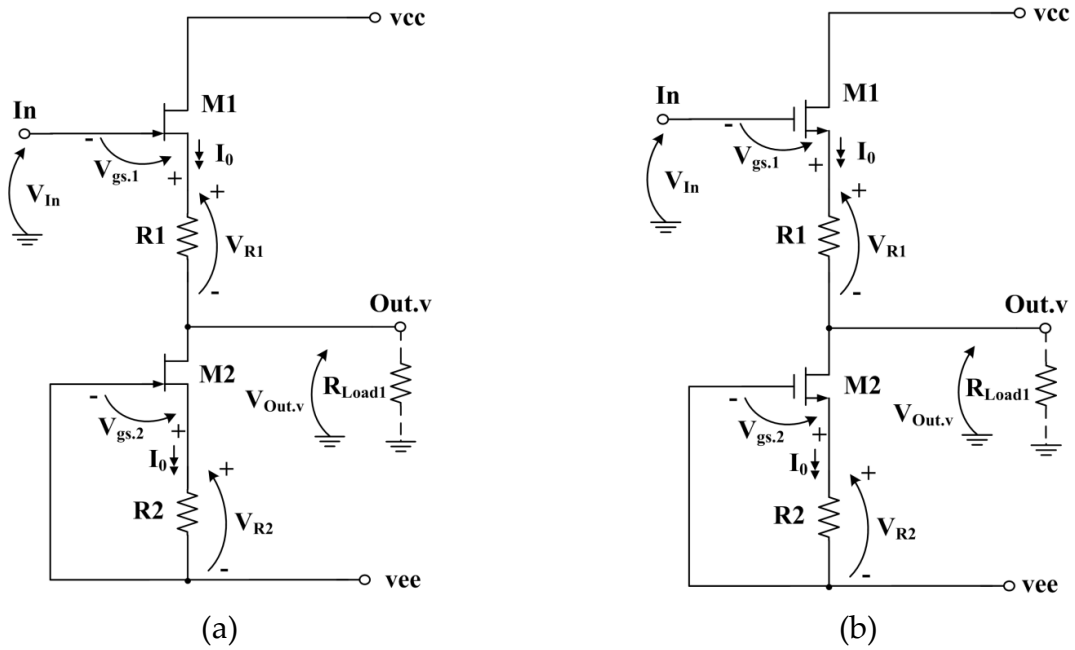

Figure 3. Buffer amplifier on JFET (a) and depletion-mode CMOS (b).

The static mode of the buffer amplifier in Fig. 3a was studied in the ADS environment on EE_HEMT transistors (Fig. 4), as well as on JFET_PFET (Fig.5) at R1=R2 =100 kΩ and a supply voltage of ±10 V.

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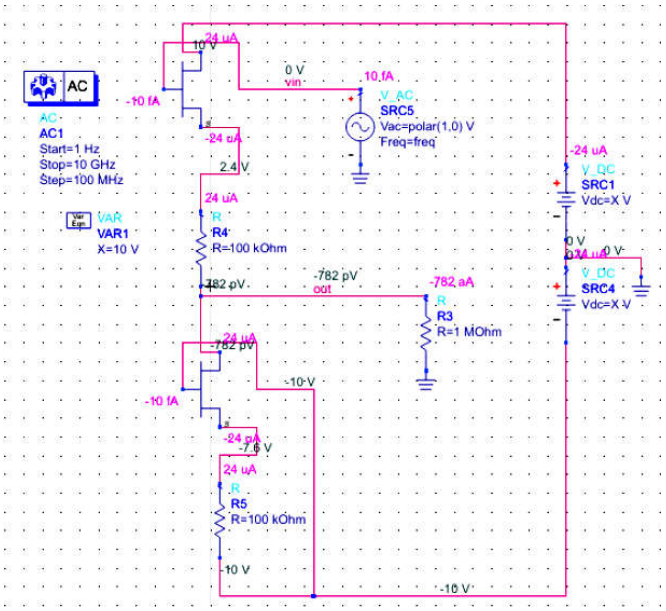

Figure 4. Static mode of the BA in Fig. 3.1a on EE_HEMT transistors.

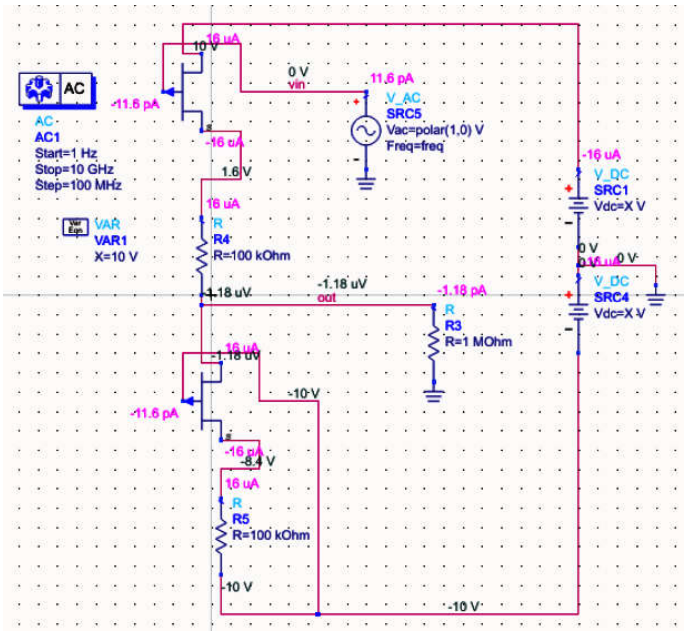

Figure 5. Static mode of the BA in Fig. 3.1a on JFET_PFET transistors.

The simulation results showed that the BA circuit in Fig. 4, when implemented on various modifications of GaN transistors, provides sufficiently low values of the offset voltage's systematic component (up to 1.18 μV). At the same time, it should be taken into account that due to the peculiarities of GaN, in some cases, BA transistors have non-zero gate currents.

The BA in Fig. 5 modeling was made in the OrCAD environment (Fig. 6) on 018NMOS transistors (JSC "Integral", Minsk, Belarus), which operate in the depletion-mode mode at R3=R4=1kΩ and a supply voltage of 5V.

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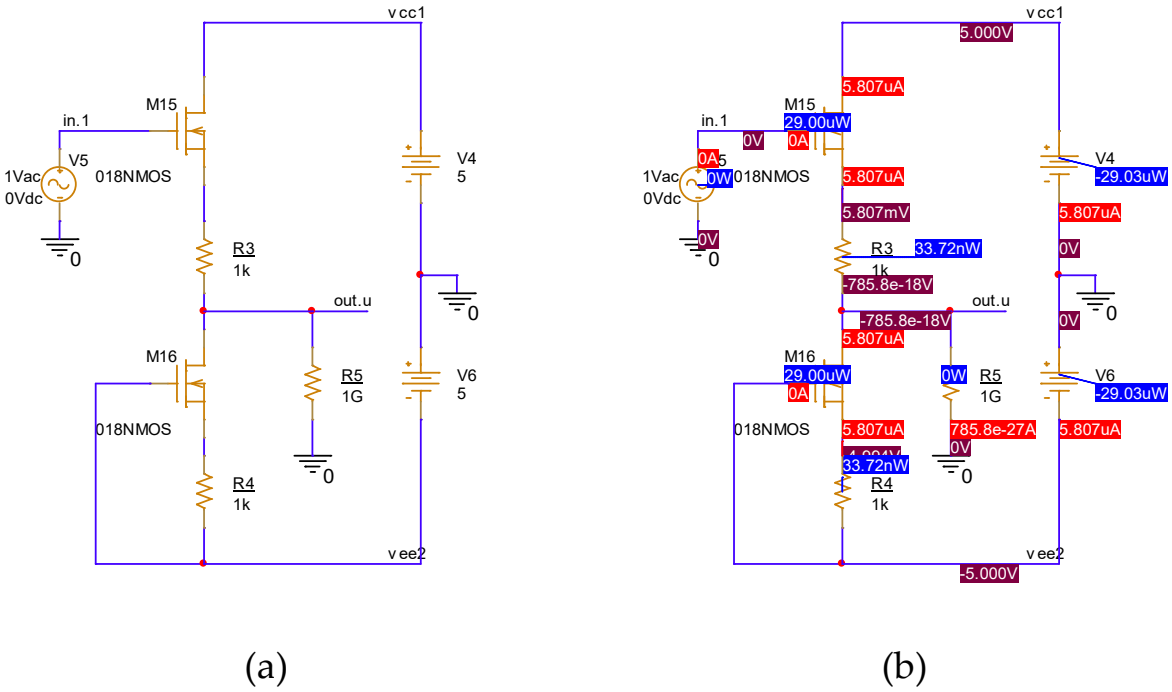

Figure 6. Depletion-mode MOS buffer amplifier by JSC "Integral" (Minsk, Belarus).

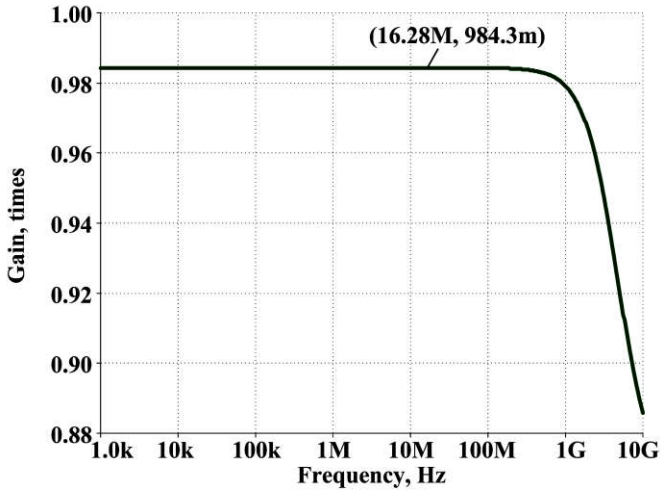

Figure 7. Amplitude-frequency characteristic of the gain of the depletion-mode CMOS BA in Figure 6.

4. Microwave GaAs JFET buffer amplifier and its switching circuit in the Sallen-Key low-pass filter structure

The circuit of an anti-aliasing low-pass filter based on the considered JFET buffer amplifier (Fig. 3a) is shown in Fig. 8. Identical JFET transistors are used here as input field effect transistors M1 and M2. The resistances of resistors R3, R4 are chosen identical. The considered circuitry of the BA makes it possible to obtain small values of the static error at the output of the low-pass filter when it is implemented both on medium-frequency Si CJFET and on GaAs microwave transistors. The developed method for constructing a low-pass filter on the proposed BA allows reducing the static error of the low-pass filter when it is turned on at the input of the ADC.

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Under the condition of manufacturing ideal leakage current frequency-setting capacitors C_1 and C_2, as well as at $V_{In}=0$, $R_{Load}\rightarrow\infty$ and zero input current of the buffer amplifier, the low-pass filter zero bias voltage is calculated by the formula:

$$V_{off} = -I_{g.1}(R_1 + R_2) + U_{gs.1} - R_3 I_0 \quad (1)$$

where $I_{g.1}$ is the gate current of the input field effect transistor M1, I_0 is the static current of the reference current source (RCS), $U_{gs.1}$ is the gate-source voltage of the M1.

Moreover, the static current of the reference current source RCS is equal to:

$$I_0 = \frac{V_{gs.2}}{R_4} \quad (2)$$

where $V_{gs.2}$ is the gate-source voltage of the FET M2 at $I_s=I_0$, R_4 is the resistance of the resistor R4.

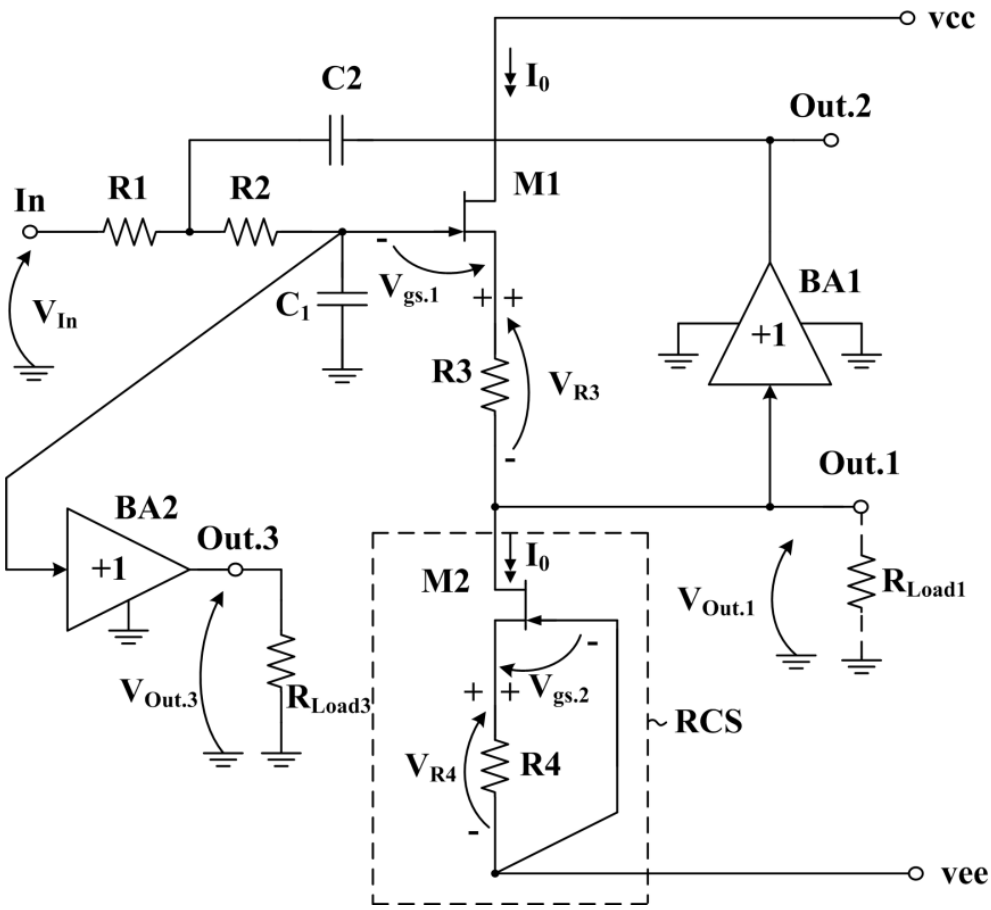

Figure 8. LPF based on JFET buffer amplifier (Fig. 3.1a).

Thus, the equation for V_{off} of the LPF in Fig. 4.1 can be summarized as:

$$V_{off} = -I_{g.1}(R_1 + R_2) + V_{gs.1} - \frac{R_3}{R_4} V_{gs.2} \quad (3)$$

From equation (3), it can be established that with a high identity of the depletion-mode CMOS transistors M1 and M2, as well as the same resistors R3 and R4, the offset voltage's systematic component of the low-pass filter (Fig. 8) is close to zero

$$V_{off} = -I_{g.1}(R_1 + R_2) \approx 0 \quad (4)$$

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On Fig. 9 shows the static mode of the LPF (Fig. 8) in the LTSpice simulation environment on microwave GaAs field-effect transistors by Minsk Research Institute of Radiomaterials at a temperature of 27°C, resistors R1=R2=50Ω, R3=R4=1kΩ, R_{Load}=R_n=1MΩ, capacitors C_1=C_2=1pF.

From the consideration of Fig. 9 it follows that the offset voltage's systematic component of the low-pass filter takes on extremely low values (450 nV).

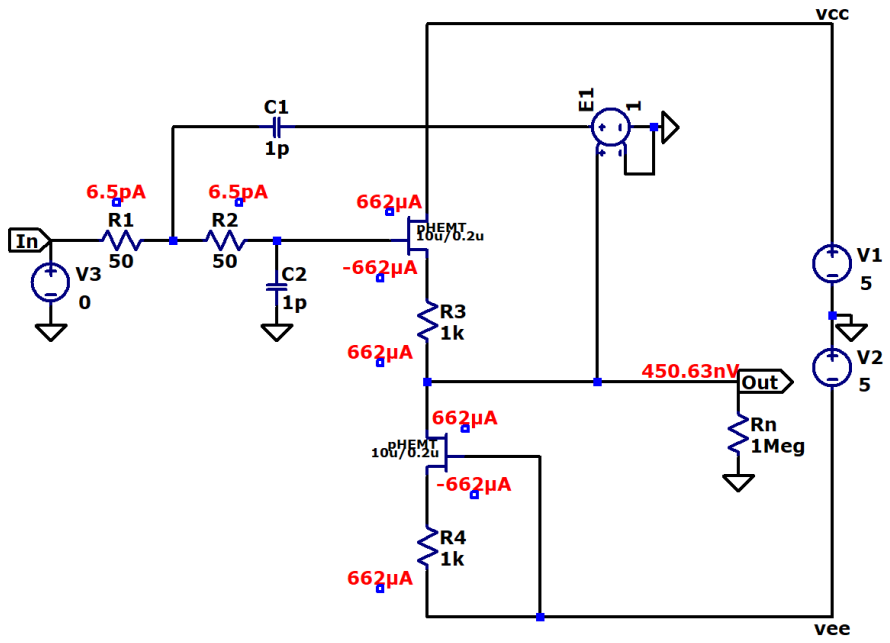

Figure 9. LPF (Figure 8) static mode in the LTSpice simulation environment on microwave GaAs JFET field-effect transistors by Minsk Research Institute of Radiomaterials.

Fig. 10 shows the logarithmic amplitude-frequency characteristic (LAFC) of the microwave GaAs LPF (Fig. 9) at 27°C.

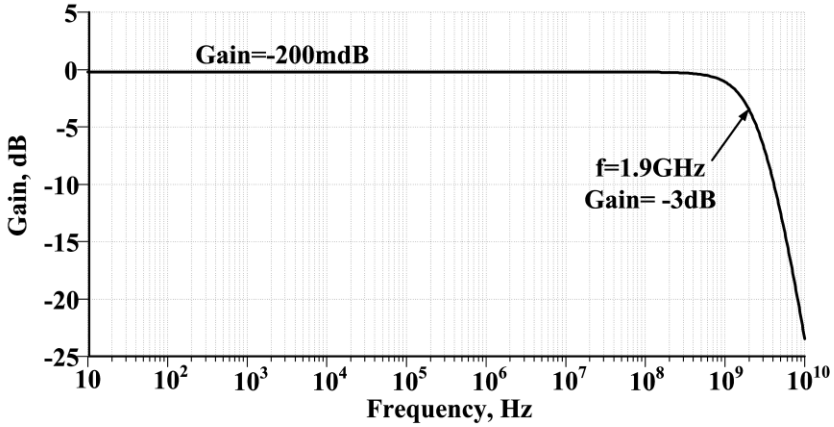

Figure 10. Logarithmic amplitude-frequency characteristic of the LPF in Figure 9.

5. Circuit for switching of the buffer amplifier on depletion-mode MOS input transistors in an operational amplifier

The circuit of the precision OpAmp [8,9], which, with 100% negative feedback, can be used as a voltage follower when designing a Sallen-Key low-pass filter, is shown in Fig. 11. A low level of the offset voltage's systematic component and increased values of the voltage gain are provided in this OpAmp circuit due to the high self-adjusting symmetry of the static mode in terms of drain currents and gate-drain voltages of the applied field-effect transistors.

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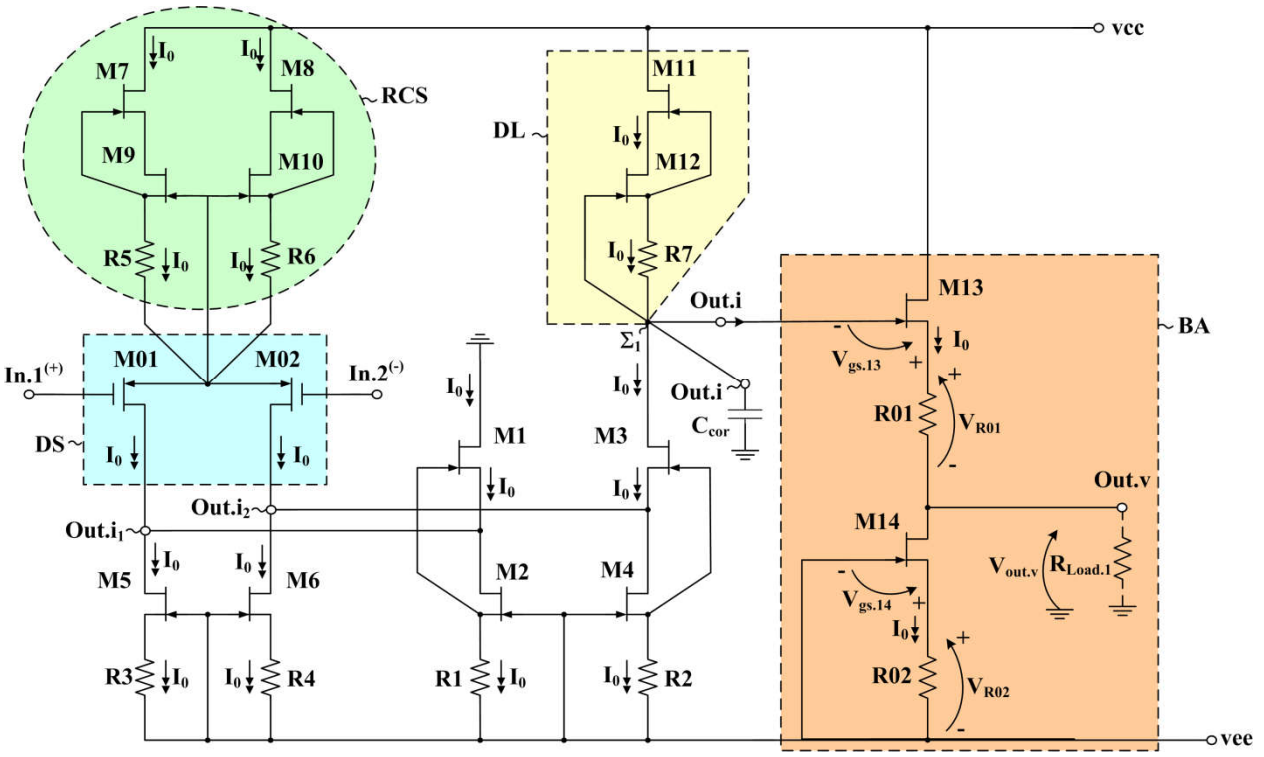

Figure 11. Low-temperature OpAmp based on BA (Fig. 3.1a), depletion-mode MOS and "folded" cascode (M1, M3).

The feature of the circuit in Fig. 11 is to create conditions under which the current output Out.i provides full mutual compensation of the static current of the dynamic load (DL) and the drain current of the field effect transistor M3. This condition is met by special construction of the reference current source (RCS), which sets the static mode of the input DS based on two parallel-connected elementary reference current sources on field-effect transistors M7÷M10, as well as the introduction of additional reference current sources on field-effect transistors M5, M6 in "folded" cascode (M1, M3). CMOS OpAmp stability Fig. 11 is provided by a correction capacitor C_{cor}.

The offset voltage's systematic component of the OpAmp (Fig. 11) [8,9] can be estimated by

$$V_{off} \approx \Delta I_{out.i} \cdot g_{\Sigma}^{-1} = \Delta I_{out.i} \cdot \left(\frac{1}{2} g_{in} \cdot A_{i3}\right)^{-1} \quad (5)$$

where $\Delta I_{out.i}$ is the output error current of the OpAmp for the current output Out.i (the difference between the static currents of the dynamic load DL and the drain current of the field effect transistor M3 at zero input differential voltage v_{diff} of the OpAmp); g_{Σ} is the conversion rate of the input differential voltage v_{diff} OpAmp into the output current of the current output Out.i; $g_{in}=g_{01}=g_{02}$ is the steepness of the drain-gate characteristic of the input field-effect transistors M01 and M02 of the input differential stage DS; $A_{i3}\approx 1$ is the current transfer coefficient of the source of the field-effect transistor M3.

The current I_{RCS} of the common source circuit Out.i_2 of the input differential stage DS, as well as the drain currents of the FETs M2÷M7, are determined by:

$$I_{RCS} = I_{R5} + I_{R6} = \frac{V_{gs.9}}{R_5} + \frac{V_{gs.10}}{R_6},$$

$$I_{R7} = \frac{V_{gs.12}}{R_7},$$

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$$I_{d6} = \frac{V_{gs.6}}{R_4},$$

$$I_{d5} = \frac{V_{gs.5}}{R_3},$$

$$I_{d2} = \frac{V_{gs.2}}{R_1},$$

$$I_{d4} = \frac{V_{gs.4}}{R_2},$$

where $V_{gs.ij}$ is the gate-source voltage of the *ij*-field-effect transistors at the operating point I_0; I_{Rn} is static current in the *n*-th resistor; R_n is the resistance of the *n*-th resistor.

The static output current of the current output error Out.i, which determines V_{off}, is equal to the difference

$$\Delta I_{out.i} = I_{DL} - I_{d3}$$

where $I_{DL}=I_7$ is the current in the resistor R_7, $I_{d3} = I_{d4} + I_{d6} - (I_{RCS}/2)$ is the drain current of the field effect transistor M3, I_{RCS} is the current of the common source circuit Out.i_2 of the input differential stage DS.

At that

$$I_{d3} = \frac{V_{gs.4}}{R_2} + \frac{V_{gs.6}}{R_4} - \frac{V_{gs.9}}{2R_5} - \frac{V_{gs.10}}{2R_6}$$

If we assume that all field-effect transistors are identical and operate at a drain current equal to some given value of I_0, which is provided by the same resistances in the circuit, then we can find

$$I_{d3} = I_0 + I_0 - \left(\frac{I_0}{2} + \frac{I_0}{2}\right) = I_0,$$

$$I_{R7} = I_{DL} = \frac{V_{gs.12}}{R_7} = I_0,$$

$$\Delta I_{out.i} = I_{DL} - I_{d3} = 0$$

Thus, with identical resistors and identical drain-gate characteristics of the applied field-effect transistors, the output error current for OpAmp (Fig. 11) [8,9] is equal to zero ($\Delta I_{out.i}=0$). As a consequence, based on equation (1), it can be found that the offset voltage's systematic component of the proposed OpAmp is also close to zero.

Open loop voltage gain OpAmp (Fig. 11) [8,9] is determined by the following equation

$$GAIN_{OL} = g_{\Sigma} \cdot R_i \quad (6)$$

where R_i is the equivalent output resistance in the current output circuit Out.i, the numerical values of which are determined by the parallel connection of the resistance of the dynamic load DL, the output resistance of the field effect transistor M3 and the input resistance BA:

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$$R_i = \frac{R_{DL} \cdot R_{CM3}}{R_{DL} + R_{CM3}} = \frac{\frac{R_7}{\mu_{11} \cdot \mu_{12}} \cdot \frac{R_{s3}}{\mu_3}}{\frac{R_7}{\mu_{11} \cdot \mu_{12}} + \frac{R_{s3}}{\mu_3}} \quad (7)$$

where R_{s3} is the equivalent resistance in the source circuit of the transistor M3, $\mu_i \approx 10^{-3} \div 10^{-5}$) is the internal feedback coefficient of the *i*-th field effect transistor in the common gate circuit, due to modulation of its length channel when the gate-drain voltage changes.

On Fig. 12 shows that the input transistors of the OpAmp operate in microamp mode, and the total current consumption (I_{cons}) of the circuit is 313.24 μA. In this case, the sources of reference currents and the output buffer amplifier are made on n-channel JFET transistors.

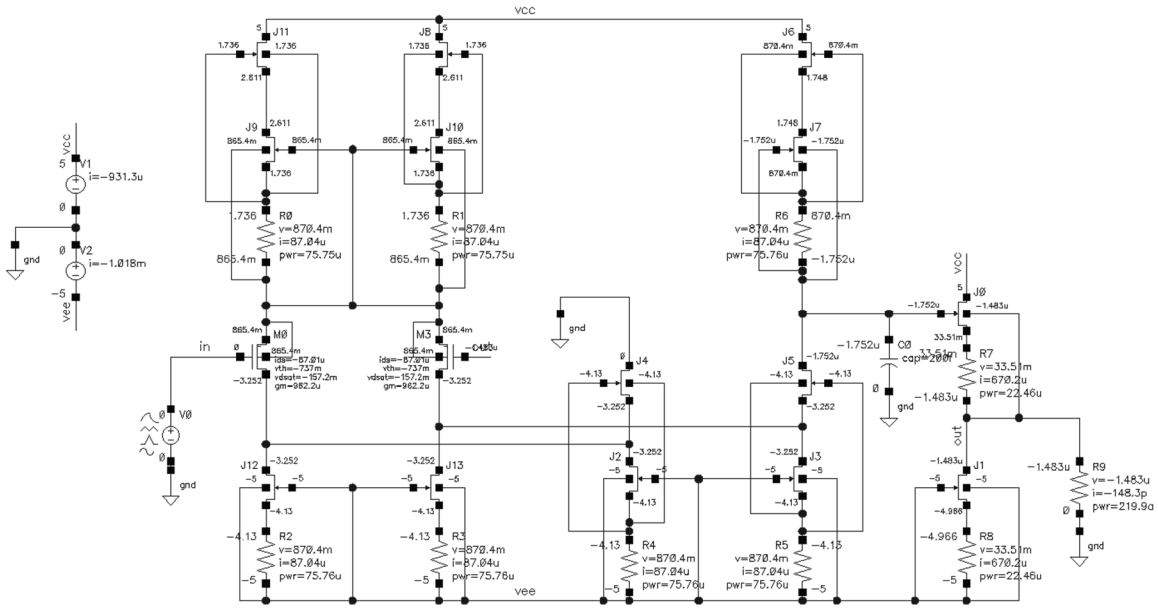

Figure 12. Static mode of the OpAmp circuit (Figure 11) in Cadence CAD environment.

The LAFC gain OpAmp Fig. 12 and its dependence of the offset voltage's systematic component on temperature are shown in Fig. 13 and Fig. 14 respectively.

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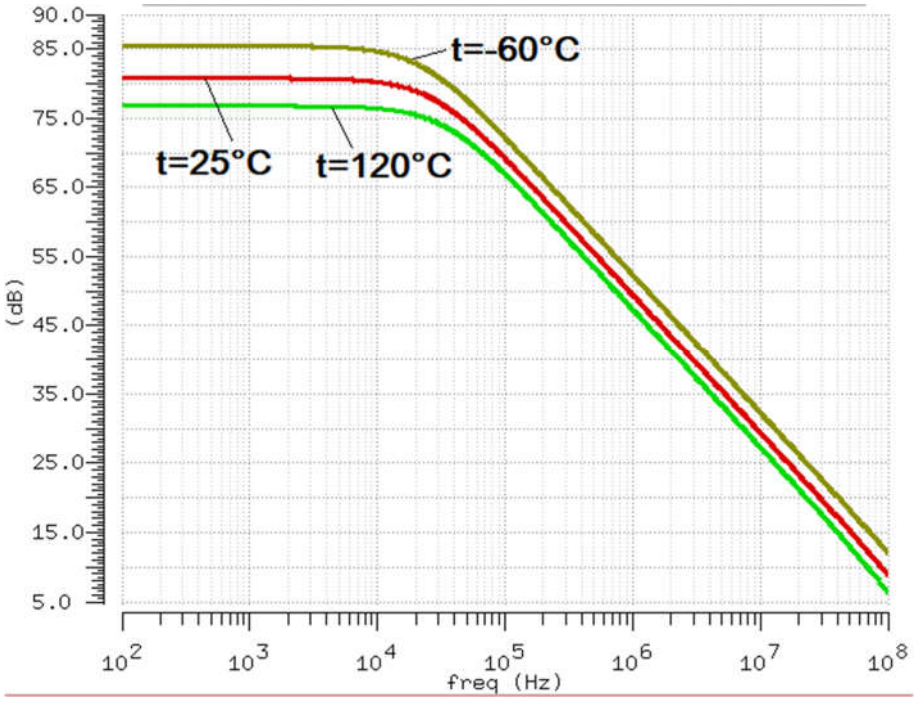

Figure 13. Open-loop gain LAFC of the OpAmp in Figure 12 at t=-60°C; 25°C; 120°C.

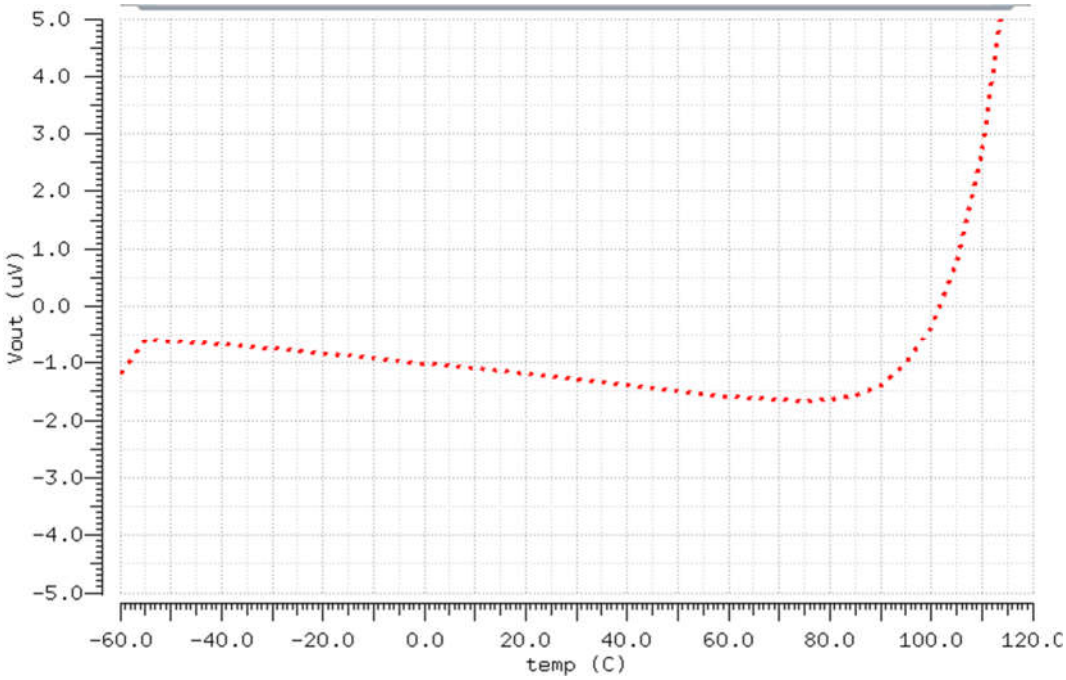

Figure 14. Dependence V_{off} of the OpAmp in Figure 13 on temperature.

6. Conclusion

In the article, buffer amplifiers (BA) were studied for the design problems of Sallen-Key class anti-aliasing low-pass filters, which are characterized by low static currents, as well as an average and extremely low offset voltage's systematic component (V_{off}). The proposed BA circuits are distinguished by a small number of elements and allow operation in the range of cryogenic temperatures, and due to the use of transistors by JSC "Integral" (Minsk, Belarus) they are operable when exposed to penetrating radiation. Control circuits based on GaAs, GaN depletion-mode CMOS and JFET technological processes have been studied. The simulation results showed that the GaN BA, when implemented on various modifications of MOS and depletion-mode MOS transistors, provides

sufficiently low values of the offset voltage's systematic component (less than 2 μV). The proposed approach to designing a microwave GaAs JFET buffer amplifier makes it possible to obtain small values of the static error at the output of a low-pass filter when it is implemented both on mid-frequency Si CJFET and on GaAs microwave transistors. This has a positive effect on reducing the error of the anti-aliasing low-pass filter when it is turned on at the input of the ADC. An example of the inclusion of the proposed control unit in the JFET OpAmp structure based on the depletion-mode MOS input stage and the "folded" cascode, which has an open-loop voltage gain equal to 76÷85 dB, and its V_{off} is within 7 μV in the temperature range from -60 ° C up to +120°C. The considered circuitry of the control unit, as well as the operational amplifier when it is turned on in the voltage follower mode, is focused on the tasks of designing active RC filters of the Sallen-Key family.

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