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Article

In-place Characterization of On-state Voltage for SiC MOSFETs: Controlled Shoot-through vs. Film Heater

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Abstract: The on-state voltage of MOSFETs is a convenient and powerful temperature-sensitive electric parameter (TSEP) to determine the junction temperature, thus enabling device monitoring, protection, diagnostics and prognostics. The main hurdle in the use of the on-state voltage as a TSEP is the per-device characterization procedure, to be carried out in a controlled environment, with high costs. In this paper we compare two novel techniques for MOSFET junction temperature estimation: controlled shoot-through and direct heating by resistive heaters embedded in two Kapton (polyimide) films. Both allow in-place characterization of the TSEP curve with the device mounted in its final circuit and assembly, including the working heat sink. The two methods are also validated against the conventional procedure in a thermal chamber.

Keywords: on-state voltage, TSEP, junction temperature, model calibration, pulsed measurements

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1. Introduction

The current trends in power electronic converters are geared towards continued improvements in key performance areas such as power density, efficiency, reliability, support to diagnostics and prognostics, and behavioral stability regardless of environmental conditions.

The boundaries of safe operating areas (SOAs) for power devices are, for the most part, determined by thermal limits. Dynamic current derating can be employed at high temperatures to ensure the best trade-off between performance and safe operation [1]. Given the ever-present pressure towards improving the performance of power electronic converters, perfect knowledge of power devices' junction temperatures would allow pushing the operating points to the limits of SOAs [2], especially during thermal cycling operation [3], to the benefit of power density, or to strike the optimal balance between performance and durability, if reliability statistics are known [4].

The junction temperature cannot be directly measured, therefore it needs to be estimated starting from suitable temperature sensitive electrical parameters (TSEPs).

As far as silicon (Si) and silicon carbide (SiC) MOSFETS are concerned, TSEPs include but are not limited to the on-state resistance, on-state drain to source voltage, threshold voltage, gate voltage plateau, body diode voltage, drain current time derivative [5,6].

Regardless of the TSEP used, the dispersion of parameters, both among the devices themselves and due to variations in the mounting of the devices in their final assemblies, makes it necessary to calibrate the systems on a per-device basis. The usual procedure calls for characterization of the devices in a thermal chamber or on a dedicated hot plate. This latter technique is used in the laboratory [7], but is impractical for production systems due to high cost.

In this work the traditional $R_{ds,on}$–T_j calibration on a per-device basis in a thermal chamber is compared with two in-place, or in-circuit, techniques. The first one has already been introduced in [8] and is based on the controlled shoot-through technique (CST). The second, entirely novel procedure uses a resistor embedded between two Kapton® (polyimide) films, working both as heating medium and temperature sensor. An example of this kind of device is given in Figure 1.

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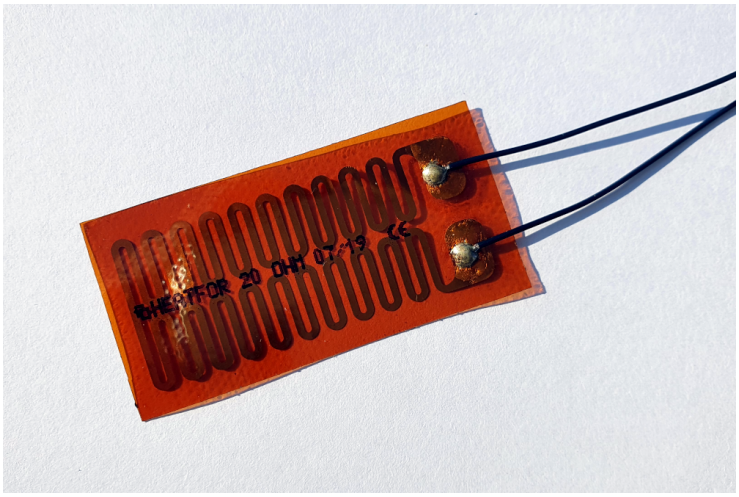

Figure 1. An example of a film heater with the RTD embedded between two Kapton® (polyimide) films.

Both in-place techniques rely on measuring the on-state drain-source voltage characteristics during the cooling phase, after a heating transient obtained without external heat. With the CST it is possible to heat the power device from the inside, by increasing its power loss independently of the load, thus even in no-load conditions. The CST also allows to let the measuring current flow during the cooling phase, even in the absence of a load. To exploit this technique, a temperature sensor must be mounted on the device case; an inexpensive NTC thermistor linearized in hardware by a proprietary circuit and algorithm is chosen here [9].

The Kapton film heater has a four-fold function: *(i)* it provides electrical insulation between the device back side and the heat sink; *(ii)* it allows a proper thermal flow from the device to the outside; *(iii)* it allows heating the device to perform the first phase of the calibration process; *(iv)* it directly measures the device case temperature.

The three techniques cited above are summarized and compared in Table 1, where their degree of maturity is also described.

Table 1. Summary of the calibration techniques compared in this paper. DUT is the Device Under Test, CD is its Complementary Device in the half bridge.

Calibration technique	Heating	Current flow	Sensor	Maturity
Thermal chamber	Ambient	Load	TC	established
CST	CST on DUT	CST on CD	Linearized NTC	recent
Kapton film	Film heater	Load	Heater as RTD	novel

The paper is structured as follows. In Section 2, the reason for choosing on-state resistance as a viable TSEP for in-place characterization is given, together with the description of the three methods presented: traditional thermal chamber calibration with pulsed current measurement, CST-based characterization and heating film characterization. The results are presented and described in Section 3, and subsequently discussed and compared in Section 4. Conclusions are drawn in Section 5. All the symbols used are defined in Appendix A.

2. Materials and Methods

2.1. On-state drain-source voltage as a TSEP

The on-state resistance $R_{ds,on}$ of a MOSFET is a reliable and fairly easy-to-use TSEP [5]. The relationship between $R_{ds,on}$ and the device junction temperature T_j can be described, in first approximation, by the Shichman-Hodges model. The current in linear (i_d) and saturation ($i_{d,sat}$) regions is, respectively,

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$$i_d = \frac{\beta}{2}\left[2(v_{gs} - V_T)v_{ds} - v_{ds}^2\right] \tag{1}$$

$$i_{d,sat} = \frac{\beta}{2}(v_{gs} - V_T)^2 \tag{2}$$

Solving (1) for v_{ds} and using (2), the on-state voltage $v_{ds,on}$ is obtained as

$$v_{ds,on} = (v_{gs} - V_T)\left(1 - \sqrt{1 - i_d/i_{d,sat}}\right) \tag{3}$$

Equation 3 is further simplified by approximating the square root with its first-order Taylor expansion, considering that for practical devices $i_d \ll i_{d,sat}$:

$$v_{ds,on} \approx \frac{i_d(v_{gs} - V_T)}{2i_{d,sat}} \tag{4}$$

The on-state resistance is obtained dividing (4) by the drain current:

$$R_{ds,on} = \frac{v_{ds,on}}{i_d} \approx \frac{v_{gs} - V_T}{2i_{d,sat}} = \frac{1}{\beta(v_{gs} - V_T)} \tag{5}$$

Despite its simplicity and the approximation, (5) is quite accurate. In fact, the choice of a specific chip carrier (package) imposes a limit on the maximum power loss that can be dissipated by the device (P_{max}). Consequently, the conduction loss must be lower than the fraction $(1 - r)P_{max}$, where r is the loss distribution coefficient (LDC), describing the ratio between switching power loss and total device loss [10]:

$$R_{ds,on}i_d^2 < (1 - r)P_{max} \tag{6}$$

which can be rewritten as

$$\frac{i_d}{i_{d,sat}} < \sqrt{\frac{4(1 - r)P_{max}}{\beta(v_{gs} - V_T)^3}} \tag{7}$$

Since both P_{max} and β scale with the semiconductor (and package) area, their ratio is approximately constant. v_{gs} is set based on driving purposes and ranges from 10 V to 20 V; with these values, we get $i_d/i_{d,sat} \ll 1$ for a broad range of devices, as shown for several commercial parts in Table 2. To compile this table, the nominal drain current is computed as

$$i_d = \sqrt{\frac{\Delta T}{4R_{th,jc}R_{ds,on}}} \tag{8}$$

$\Delta T = 70\,^{\circ}\mathrm{C}$ is a common overtemperature for power devices; this value is divided by the total thermal resistance of the device to the ambient, approximated as $2R_{th,jc}$, considering the total value to be equally shared between the device and the thermal interface material. Another factor of two descends from $r \approx 1/2$. $i_{d,sat}$ is assumed to coincide with the maximum pulsed drain current.

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Table 2. Values of the ratio $i_d/i_{d,sat}$ for some commercial parts. The values, largely smaller than one, support the applicability of the approximation (4).

Part number	Device type	Breakdown voltage [V]	Package	$i_d/i_{d,sat}$
STW77N65M5	Si MOSFET	650	TO-247-3	0.150
IPW65R022CFD7A	Si MOSFET	650	TO-247-3	0.107
IPP65R050CFD7A	Si MOSFET	650	TO-220	0.126
C2M0080120D	SiC MOSFET	1200	TO-247-3	0.239
C3M0025065K	SiC MOSFET	650	TO-247-4	0.156

In this work, the experimental tests are performed on the device C2M0080120D, which is a SiC MOSFET and exhibits the largest $i_d/i_{d,sat}$ among those considered, thus representing the worst-case for the dependence of $R_{ds,on}$ on the drain current.

Equation 5 also highlights the two components affecting the dependence of on-state resistance on the junction temperature. In fact, the gain β contains the electron mobility μ_n, which decreases with temperature, while the threshold voltage V_T decreases as well, according to these empirical rules [8]

$$\beta(T_j) = k\left[A + B\left(\frac{T_0}{T_j}\right)^{\gamma}\right] \tag{9}$$

$$V_T(T_j) = V_T(T_0)\Big[1 - \alpha(T_j - T_0)\Big] \tag{10}$$

where k, A, B, α and $\gamma > 1$ are fitting constants depending on the individual device sample and material. These dependences result in two regimes in the $R_{ds,on}$–T_j characteristic: a positive temperature coefficient (PTC) regime related with mobility decrease, dominant at higher temperatures, and a negative temperature coefficient regime (NTC) connected with the decreasing threshold voltage, more relevant in a cold device. These two regions are highlighted in Figure 2. Hence, a minimum point for $R_{ds,on}$ exists; since the proposed method is based on the inversion of the $R_{ds,on}$–T_j curve, this point limits the range of applicability of the presented technique, determining the inversion range of the curve. This minimum point (T_{jF}) is obtained by deriving (5) and looking for the zero of the derivative:

$$\begin{aligned}\frac{\mathrm{d}(1/R_{ds,on})}{\mathrm{d}T_j} &= (v_{gs} - V_T)\frac{\mathrm{d}\beta}{\mathrm{d}T_j} + \beta\frac{\mathrm{d}(v_{gs} - V_T)}{\mathrm{d}T_j} \\ &= -kB\gamma T_0^{\gamma} T_j^{-(\gamma+1)}(v_{gs} - V_T) + \alpha\beta V_T(T_0)\end{aligned} \tag{11}$$

$$T_{jF} = \sqrt[\gamma+1]{\frac{kB\gamma T_0^{\gamma}(v_{gs} - V_T)}{\alpha\beta V_T(T_0)}} \tag{12}$$

It is important to note that T_{jF}, as given by (12), when computed for typical devices and driving voltages, falls around room temperature, or below. This coincides with the typical use of MOSFET in their PTC region, for thermal stability purposes, and limits the applicability of our method to temperature values above room temperature [11,12]. This "inversion region" (in mathematical sense), where our method can be applied, is represented by the blue line in Figure 2.

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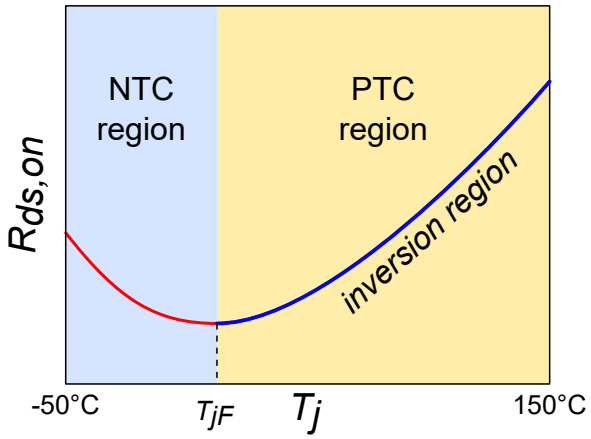

Figure 2. Typical $R_{ds,on}$–T_j curve, with clearly visible NTC and PTC regions. The minimum point is at T_{jF} (see (12)); above T_{jF} the relationship can be inverted to estimate T_j from a direct on-state voltage or resistance measurement.

2.2. Thermal model of the inner layers of the power device

Power electronic devices are usually modeled with a three-time-constant RC thermal network, following the Cauer or Foster approach [13,14]. The ultimate objective of a TSEP is to determine the junction temperature, which is usually inaccessible. Nonetheless, using the aforementioned thermal model, it is possible to estimate the junction temperature under certain circumstances. A typical thermal network for a power MOSFET is given in Figure 3.

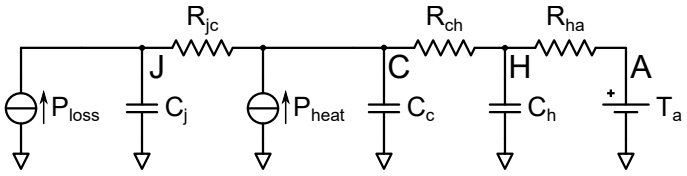

Figure 3. One-dimensional thermal network of a power electronic device connected to a heat sink. Subscripts describe the relevant thermal nodes: junction (J), case (C), heat sink (H), ambient (A).

In a typical system, the thermal resistance between junction and case (R_{jc}) is comparable with that of the thermal interface material (TIM) coupling the device case with the heat sink (R_{ch}); however, the thermal capacitance of the junction (C_j) is much lower (possibly, more than one order of magnitude) than that of the device body (C_c), which is, in turn, smaller than the capacity of the heat sink (C_h). This results in well-spaced thermal time constants.

Starting from this assumption, in stationary conditions, when the power source is the device junction itself (i.e. P_{loss} in Figure 3, as it happens in normal operation and in CST) there is a temperature difference T_{jc} between junction and case:

$$T_{jc} = T_j - T_c = P_{loss} R_{jc} \tag{13}$$

Nonetheless, when the power source is located at the case (P_{heat} in Figure 3, such as in the case of the film heater) or beyond it (heat sink or cooling to ambient temperature), the fast time constant of the junction $\tau_j = R_{jc} C_j$ implies that the junction and the case are almost at thermal equilibrium. In this case, it is possible to infer the junction temperature by a sensor placed on the device case.

2.3. Low-cost sensor conditioning

Both the in-place characterization procedures presented in this work rely on low-cost temperature sensors that can be easily added to the system without excessive economic

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penalties. These sensors are used to monitor the device case temperature during the cooling phase: once the device heating phase is completed, a thermal transient as described in Section 2.2 starts. After its completion, case and junction will be isothermal. This allows using the case sensor to determine the junction temperature. This can be done because the C_j thermal capacitance is usually small with respect to the others, and the junction is expected to be in thermal equilibrium with the case from several milliseconds after the P_{loss} source is turned off.

NTC thermistors are known for their highly non-linear behavior; to achieve an accurate yet simple conditioning, we use a proprietary linearization algorithm based on a non-linear voltage divider employing a silicon pn diode [9]. The voltage across the diode is measured and transformed in the normalized log resistance g of the NTC, having a room temperature value of R_0 and a value R_T at a generic absolute temperature.

$$g = \ln\left(\frac{R_T}{R_0}\right) \tag{14}$$

g is connected to the diode voltage v measured at the NTC-diode divider at the unknown temperature; this dependence follows the first-order-accurate equation

$$g \approx g_a + \frac{v - v_a}{v_b - v_a} \ln \frac{R_b}{R_a} \tag{15}$$

where v_a and v_b are the diode voltages corresponding to the resistance values R_a and R_b (reference resistors are temporary used in the divider in place of the thermistor) and g_a is obtained using (14) with R_a instead of R_T. The absolute temperature can be directly obtained from g using

$$T = a + bg + cg^2 + dg^3 \tag{16}$$

where coefficients a, b, c and d can be obtained by a calibration procedure or directly using the NTC resistance map provided by the thermistor manufacturer, depending mainly on the NTC material.

The heater embedded into the Kapton film is designed to dissipate power, hence it is not meant as a temperature sensing device. Nonetheless, a measurement campaign revealed that it follows a linear rule identical to resistance temperature detectors (RTDs),

$$R_F = R_{F0}\left[1 + \alpha(T - T_0)\right] \tag{17}$$

where R_{F0} is the value at room temperature, α the temperature coefficient of resistance (TCR) and T_0 the reference temperature at which R_{F0} is measured. The resistance is sensed by an ohmmeter and the linear relationship can be inverted straightforwardly.

2.4. Calibration in the thermal chamber

The TSEP calibration for a given device can be obtained by using a thermal chamber, i.e., an environment with controlled temperature, inside which the device under test can be placed. A limitation of this approach is the need to heat the power device only, avoiding overheating of the other components. This condition reflects most of the real-world power electronics, where the power switches experience the highest temperature levels.

Hence, the power device is offset from the main board by means of an appropriate cable, which allows carrying command, power and sensing signals, and placed inside the thermal chamber. The cable used is composed of six wires, to guarantee "Kelvin" connection for the most delicate quantities. Two thicker wires are used for drain and source currents, another couple is used to carry the gate signal (v_{gs}) and another pair senses the $v_{ds,on}$. The chamber is set at the desired temperature (the one for which we want to measure the $R_{ds,on}$) and, once the target temperature is reached, a current pulse (shorter than 500 µs) is fired to the device while it is on at the desired v_{gs} voltage; the $v_{ds,on}$ is then recorded.

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Using a current pulse is essential to avoid device self-heating, which could invalidate the measurement. In fact, if the current pulse is longer than the thermal time constant of the junction of the device, the junction temperature itself becomes higher than the chamber temperature, thus giving misleading results. In this work, we used exponential pulses, achieved by supplying the circuit with a capacitor of appropriate value rather than with a complete power supply. As the current starts to flow in the load resistor, the capacitor discharges. This is a simple yet fast way to record $v_{ds,on}$ at different current values, provided that a large bandwidth oscilloscope is available; $R_{ds,on}$ is then computed as the ratio $v_{ds,on}/i_d$.

In addition, since a high voltage swing occurs at the device drain as soon as it is turned on, a clamper circuit like that of [15,16] is used to guarantee sufficient resolution in the on-state voltage measurement.

To collect enough points for a TSEP characterization curve, the process is repeated at several different temperature levels; since the temperature inside the chamber is expected to be uniform in space, provided that the chamber temperature has been given a long enough time to settle, points can be collected both during the heating and the cooling transients. The process used to obtain the characterization curve in the thermal chamber is illustrated in Figure 4, while Figure 5 gives the circuit arrangement used in this experiment.

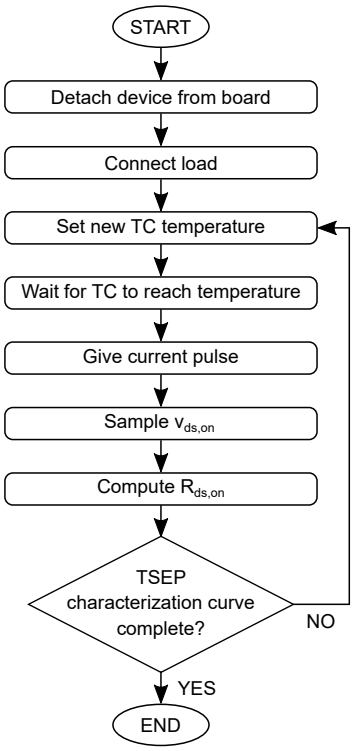

Figure 4. Flowchart of the procedure to obtain the TSEP characterization curve in the thermal chamber.

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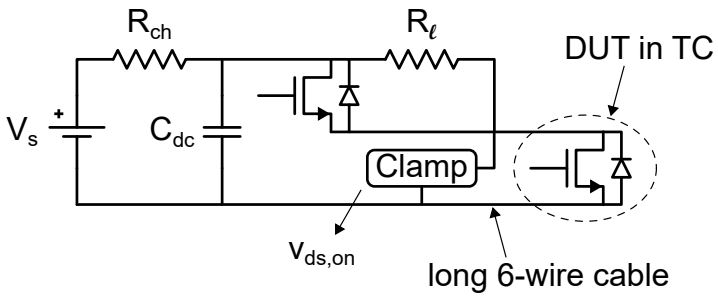

Figure 5. Schematic representation of the circuit used to measure the on-state drain-source voltage in the thermal chamber. A load is essential to let the current flow in the DUT, while the use of a capacitor instead on a DC supply allows you to capture multiple $v_{ds,on}$–i_d values in a single pulse.

2.5. Controlled shoot-through calibration

The controlled shoot-through technique allows you to selectively activate a new loss mechanism in gate-controlled power devices arranged in half-bridge configurations. When the device of interest is in off state and, consequently, its complementary device is fully on, the former can be partly turned on with a reduced gate voltage (V_{st}), low enough to be below its Miller voltage limit. This forces the device into the saturation region, i.e. with voltage-controlled current source (VCCS) behavior. The complementary device is fully on, so the drain-source voltages of both devices are unaltered, but a controlled current I_{st}, determined by properties of the devices and by the applied gate voltage, flows as a shoot-through current.

The current level can be adjusted by acting on the intermediate gate voltage V_{st}, while the overall power of the device is controlled mainly in the time domain; using period-average quantities, the power loss by CST is, in first approximation,

$$P_{st} = cV_{dc}I_{st}(V_{st}) \tag{18}$$

where V_{dc} is the DC voltage at the extreme points of the half bridge and c is the CST duty ratio, defined as the ratio of the CST pulse duration to the switching period, $c = t_{st}/T_{sw}$.

The CST power can be used to heat the device independently of the load connected to the half bridge; in fact, the CST current flows regardless of the load. Combining these two properties, it is possible to devise a TSEP characterization procedure that can occur entirely in-circuit, as described in the following and summarized in Figure 6, while the circuit is given in Figure 7. First, the DUT is heated by repeatedly firing CST pulses while the complementary device is on; then, once the maximum desired temperature is reached, the DUT is fully turned on fully and only sporadic CST pulses are sent to the CD, thus allowing the measuring current to flow.

There are two main differences between the CST and the thermal chamber approach: (1) only one current level can be set here, unless a variable V_{st} active gate driver (AGD) is used (which is not in the current setup); (2) a specific thermal sensor must be placed next to the device, to sense its case temperature: under the thermal equilibrium hypothesis, this will be also the junction temperature, if measurements are taken during the cooling transient.

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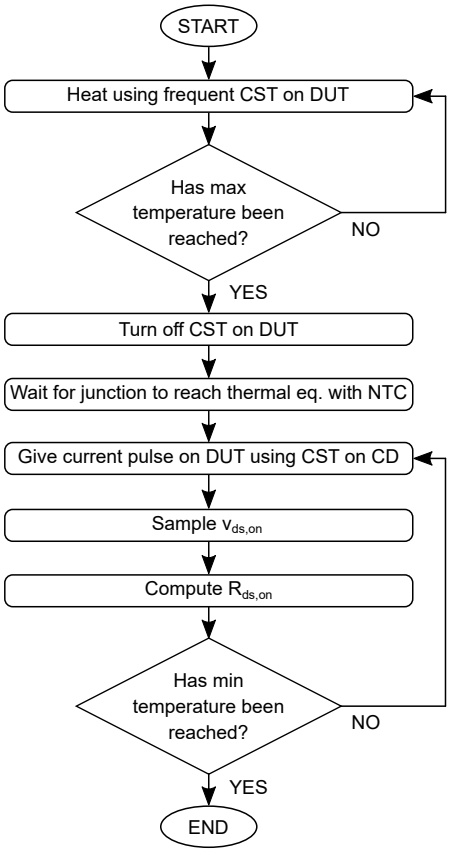

Figure 6. Flowchart of the procedure to obtain the TSEP characterization curve by exploiting CST for both heating and test current generation.

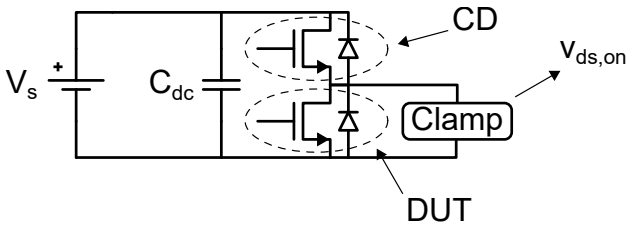

Figure 7. Schematic representation of the circuit used to measure the on-state drain-source voltage exploiting CST. There is no need for a load to be connected to the half bridge, but it is possible to detect $v_{ds,on}$ for a single $i_d = I_{st}$ current level.

2.6. Direct film heating calibration and sensing

The third and completely novel technique for the TSEP characterization presented here is based on resistive heaters embedded in Kapton films, working as both heating medium and temperature sensor with RTD behavior. The Kapton heater is mounted between the device back side and the heat sink, and fed by a separate generator.

The characterization procedure is summarized in Figure 8. Unlike in the case of the thermal chamber, the device is not taken off the board, but is retained in its normal position in the converter assembly; Figure 9 reports the circuit used for the test.

It is important to note that when moving from the heating phase to the cooling-measuring phase, the Kapton resistor needs a certain amount of time to reach thermal equilibrium with the case. As a result, its not possible to obtain reliable temperature measurements close to the transition from heating to cooling.

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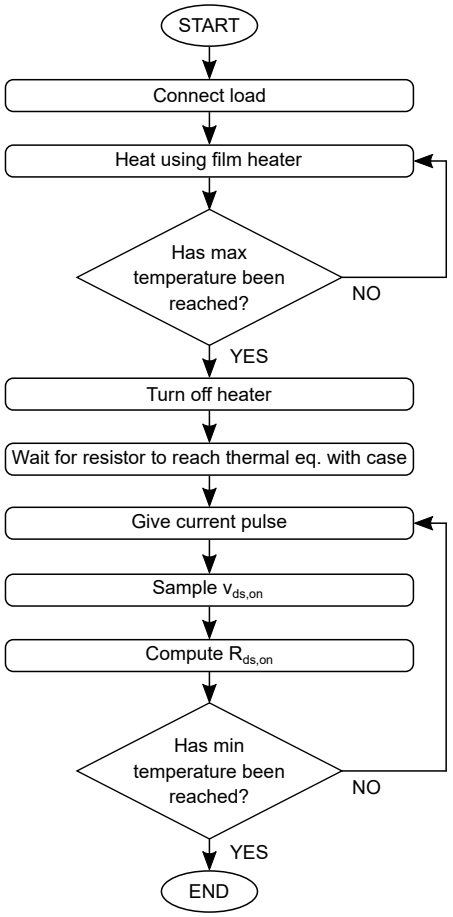

Figure 8. Flowchart of the procedure to obtain the TSEP characterization curve based on Kapton heater-sensor. A load is essential to let the measuring current flow.

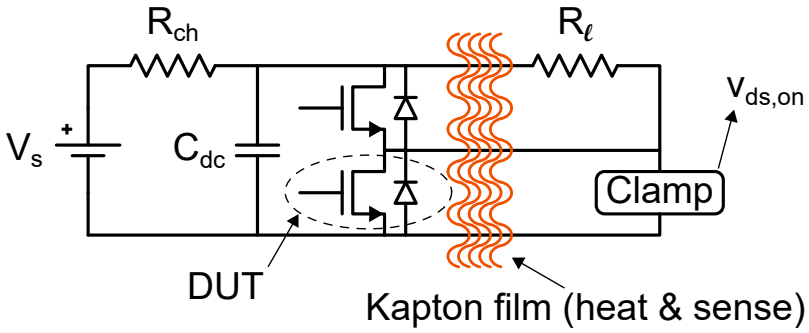

Figure 9. Schematic representation of the circuit used to measure the on-state drain-source voltage using Kapton-embedded resistor and current flow on an external load.

2.7. Experimental setup

To perform all the aforementioned tests, we used one of the legs of a custom-built three-phase converter. Three-level AGDs were connected to both the high- and the low-side devices; the two traditional levels (to turn the device on and off) are complemented by a fixed V_{st}, which can be changed at the circuit level but not at runtime.

As already stated, the Kapton film with embedded resistor is placed between the back side of the two SiC power MOSFETs and the heat sink; this prevented the possibility of screwing the devices to the sink itself, hence a pressing bar is employed to keep the devices in place. The NTC sensors used for the CST characterization procedure are placed

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between the pressing bar and the top side of the devices; this introduces significant thermal resistance between the device case and the NTC sensor: in order to take this into account, the thermal network of Figure 3 has been modified as shown in Figure 10. The whole setup is documented in the photo of Figure 11.

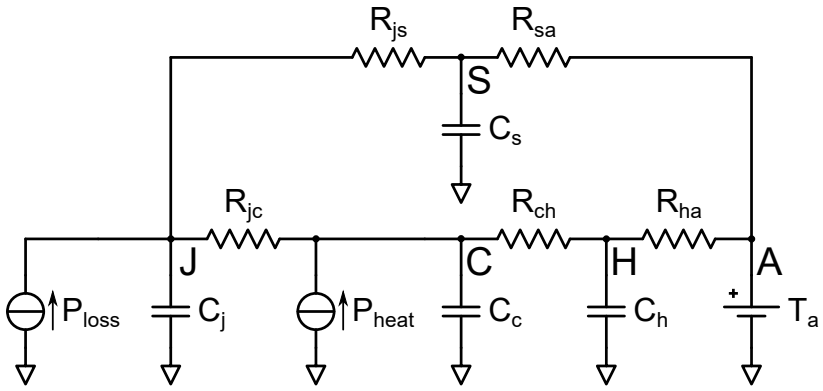

Figure 10. Thermal network of a power electronic device connected to a heat sink, with a secondary thermal path to include a NTC sensor mounted on the case top.

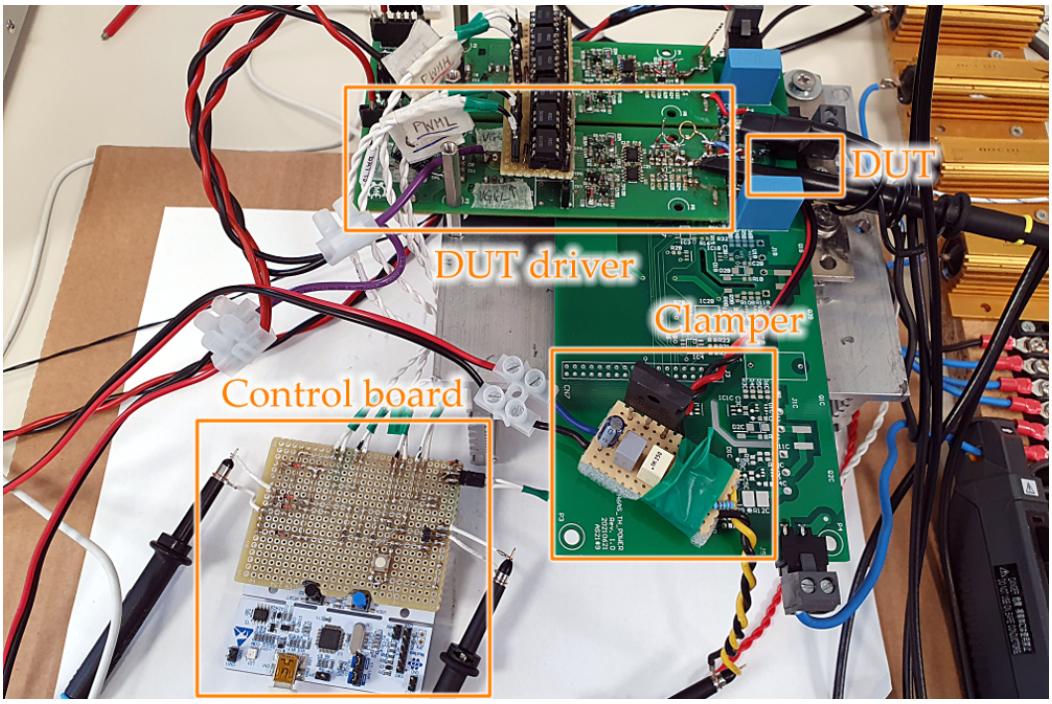

Figure 11. Experimental test bench including the three-phase bridge (out of which just a single phase is used), power devices, heat sink, Kapton-embedded heater and NTC sensors. The board on the left is an STM32 Nucleo F446, generating the control signals.

3. Results

3.1. Sensor characterization

As a first step, the sensors used for the in-place TSEP characterization (10 kΩ NTC and Kapton film RTD) were calibrated in a controlled environment, using a K-type thermocouple as a reference. The results are presented in Figure 12 (NTC) and Figure 13 (Kapton). The extracted values for the model parameters are given in Table 3.

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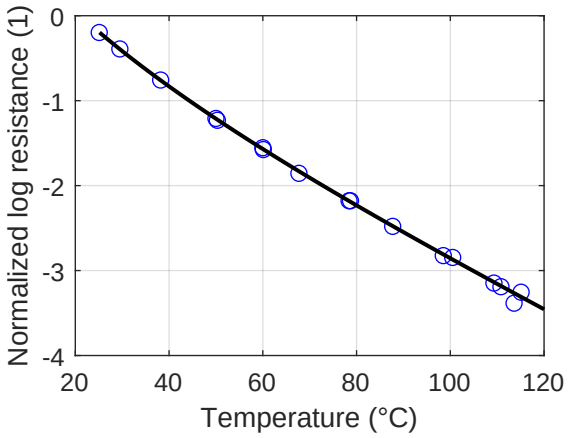

Figure 12. Calibration curve for the hardware-linearized NTC sensor. The blue circles represent the experimental points, while the solid black line denotes the fitted model (third-order polynomial).

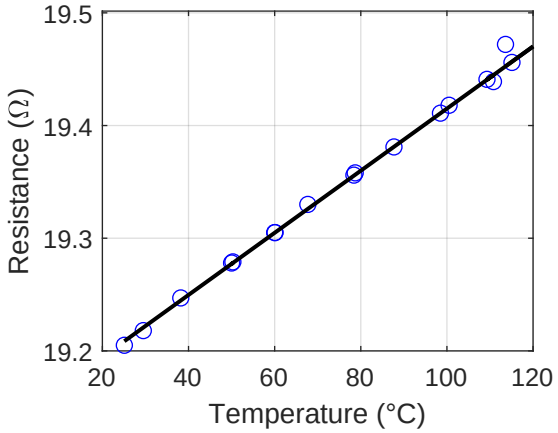

Figure 13. Calibration curve for the resistor embedded in the Kapton heater film. The blue circles represent the experimental points, while the solid black line denotes the fitted model. The purely linear model denotes the possibility to use the heater as RTD; its Temperature Coefficient of Resistance suggests that it is made of Chromel V.

Table 3. Parameters of the mathematical models (16) and (17) for the NTC thermistor and film heater used as a RTD.

Parameter	Value	Unit
a	294.2	K
b	-20.02	K
c	3.519	K
d	0.2973	K
R_{F0}	19.14	Ω
α	144 ppm	1/K

3.2. Device self-heating

A heating step can be used to characterize the time constant of the device junction. This allows to estimate an effective maximum pulse length for the $v_{ds,on}$ measurements, while guaranteeing the absence of significant junction self-heating. The results of this test are shown for short and long times, respectively, in Figure 14 and Figure 15.

From Figure 14 we can determine the junction thermal time constant to be around

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250 µs, fully consistent with the "below 200 µs" suggestion given in the datasheet of C2M0080120D for the junction thermal parameters. The initial drop in the measured $R_{ds,on}$ is related to the limited bandwidth of the clamping circuit, which needs several microseconds to settle. It is also possible to note that in the 500 µs window presented, the relative change in $R_{ds,on}$ is limited to 7.7 %.

Figure 15 describes the change in the on-state resistance for a longer observation time: it is clear that a second thermal transient exists, with a completely different time constant. This transient is believed to be related to device case heating.

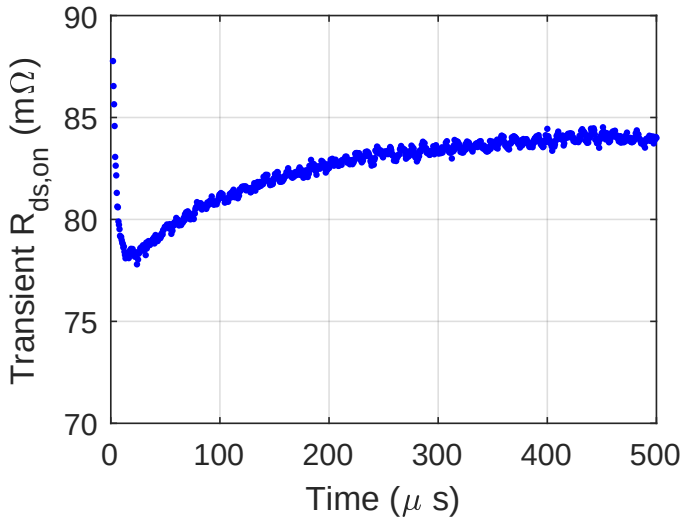

Figure 14. Junction self-heating short-term transient monitored on $R_{ds,on}$ and measured at ambient temperature under a current of 18 A.

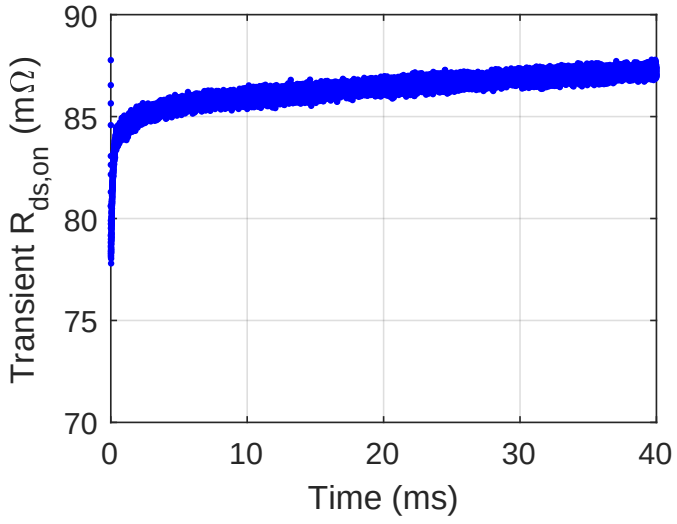

Figure 15. Junction self-heating medium-term transient monitored on $R_{ds,on}$ and measured at ambient temperature under a current of 18 A. The upward drift describes case temperature increase.

3.3. Comparison of the different measurement techniques

The TSEP characterization procedures presented in Section 2.4, Section 2.5 and Section 2.6 are applied to the same device under test and the results are collected in Figure 16 and Figure 17, while the circuit parameters are given in Table 4. The main difference between the two figures is related to the sensor used to determine the device temperature: in Figure 16, the NTC thermistor is assumed to be in thermal equilibrium with the junction, hence it

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is used to generate the "Device temperature" axis in the figure; for Figure 17, the Kapton film resistor is used as the reference thermal sensor.

The color of the curves represents the three characterization procedures, plus variants devised to get better understanding. In addition, the experimental dots are complemented by third-order polynomial fitting curves. The green dots pertain to the thermal chamber characterization, while the blue ones are those resulting from the Kapton procedure; the black dots refer to the CST-based characterization process. The other two sets of points, red and magenta, represent, respectively, thermal chamber results using long measuring pulses (i.e., with self-heating of the junction) and a hybrid procedure using the Kapton film for heating and the CST for measuring the on-state resistance.

Table 4. Parameters of the bench used for the TSEP characterization under different conditions.

Description	Parameter	Value	Unit
Supply voltage, chamber and Kapton	V_s	120	V
Supply voltage, CST	V_s	180	V
DC link capacitance, chamber and Kapton	C_{dc}	47	µF
DC link capacitance, CST	C_{dc}	560	µF
Supply output resistance	R_{ch}	100	Ω
Load resistance	R_ℓ	2.5	Ω
Device type	—	C2M0080120D	—

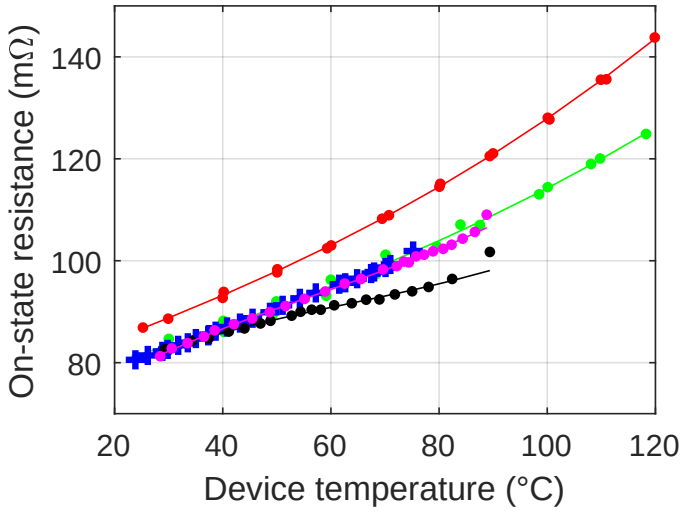

Figure 16. Experimental TSEP characterization curves obtained using different procedures: thermal chamber with long pulses (red), thermal chamber with fast pulses (green), CST heating-measure (black), Kapton heater-sensor (blue), hybrid mode with Kapton heating and CST measure (magenta). Device temperature is measured by the NTC sensor; measurements correspond to a reference current of 18 A.

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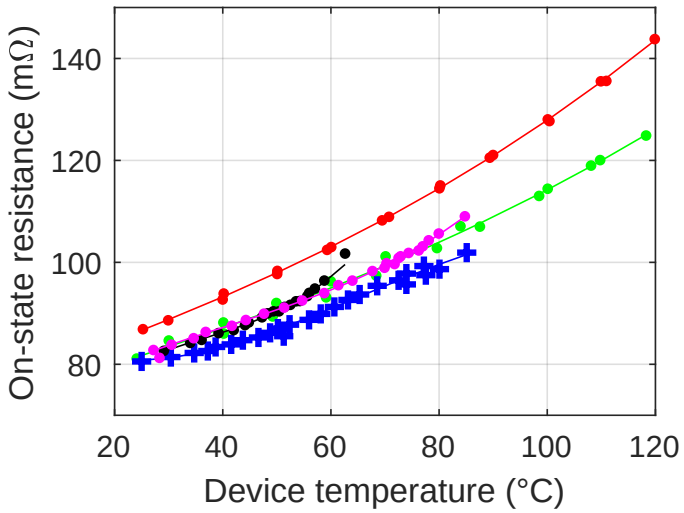

Figure 17. Experimental TSEP characterization curves obtained using different procedures: thermal chamber with long pulses (red), thermal chamber with fast pulses (green), CST heating-measure (black), Kapton heater-sensor (blue), hybrid mode with Kapton heating and CST measure (magenta). Device temperature is measured using the resistor embedded in the Kapton film; measurements correspond to a reference current of 18 A.

3.4. Long CST pulses

Equation 18 shows that a great power loss can occur when CST is used. A general guideline not to exceed device ratings is to make the maximum CST power loss similar to the switching loss. Thus, the CST time $t_{st} = cT_{sw}$ is usually in the range of microseconds or even below 1 µs. Longer pulses can dramatically fast heat the device that is undergoing the controlled shoot-through phenomenon; Figure 18 shows what happens in this condition.

As for the other experiments, the DUT is the low-side device of the half bridge. It is fully-on and its on-state voltage is represented in blue in the figure. The device undergoing CST is hence the CD, i.e. the high-side one in this test. Since no load is connected at the output, the DUT on-state voltage is zero until the CST current (in red) starts to flow; that current is identical for both DUT and CD.

It can be seen that, for time spans of several microseconds, the CST current is constant (about 17 A), then it starts to ramp up with a derivative of about 75 mA/µs. At the same time, the computed on-state resistance (in green) is constant, confirming that the DUT is not heating for short times, as already explained in Section 3.2. It is important to note that, during the CST pulse, for the CD $v_{gs} = V_{st}$, i.e. the gate is kept at constant voltage V_{st}.

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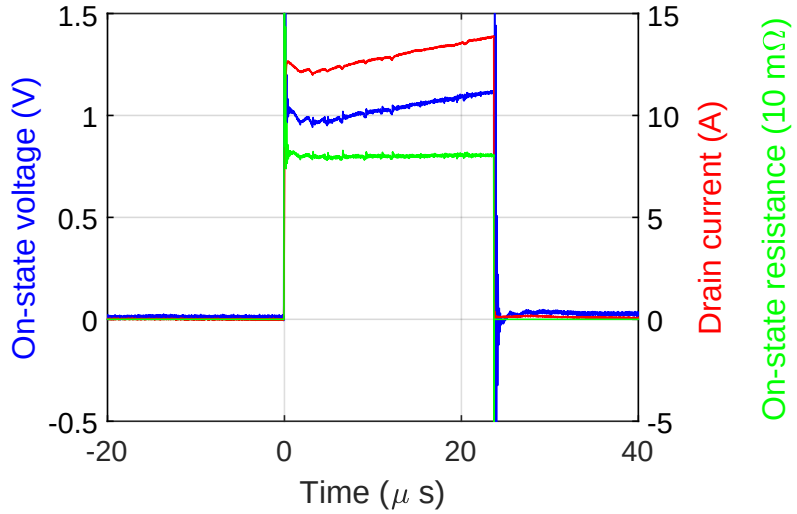

Figure 18. Transient response of the half bridge under a 25 µs-long CST pulse on its high-side device, with the low-side one fully on. The drain current of both high-side and low-side devices is in red, while the on-state voltage of the low-side one is in blue; the computed on-state resistance is in green.

4. Discussion

The results of Section 3.1 suggest that both a properly conditioned NTC and a polyimide-embedded resistive heater can profitably be used as cost-effective and reliable temperature sensors, in support of the in-place characterization procedure. The resistive heater is, as expected, a real RTD; as such, it exhibits excellent linearity but also the drawback of poor sensitivity, as denoted by a TCR of just 144 ppm. With respect to standard RTDs, such as Pt100 and Pt1000, there is the disadvantage of low resistance value, which is optimized for heating rather than for sensing (around 20 Ω in this setup), which makes it even more challenging to properly condition in embedded circuits, rather than in full-fledged sensing setups.

The NTC thermistor, when linearized by the proprietary hardware circuit used here, still presents good linearity, even if third-order polynomial functions are needed to guarantee good accuracy. Nonetheless, qualification of the temperature sensor accuracy is outside the scope of the present work. The results achieved show the possibility to obtain a higher SNR with the NTC sensor, given its higher sensitivity; this is an important property considering the final use of this sensors in electromagnetically noisy environments, as those typical for power electronic converters.

Section 3.2 gives relevant insights of the process of junction self-heating and also highlights an experimental way to characterize the device thermal capacitance. In fact, when it comes to power devices, it is common to acquire clear and reliable thermal resistance values, as it happens for R_{jc} (usually given by the device manufacturer), R_{ch} (retrievable from the TIM properties and mechanical data) and R_{ha} (provided by the heat sink manufacturer). The same thing does not hold for thermal capacitance, which is largely unknown. With the use of TSEP as presented here, it is possible to obtain visually-separated thermal time constants, and compute the thermal capacitance value as the ratio of the measured time constant to the given thermal resistance. It is worth noting that, since the time constant is a ratio-based measurement, no TSEP calibration is needed, thus considerably simplifying the process.

Figure 14 gives two other important pieces of information. First, the bandwidth of the clamper for the $v_{ds,on}$ measurement must be tightly controlled: the steep transient in the 0 µs to 10 µs range is due to the time needed by the clamper to reach its steady-state value. This is important only if the $v_{ds,on}$ measurement occurs near the switching edge, as it is common for standard load-based current pulse generation (as for thermal chamber and Kapton procedures); the CST approach on the other hand is immune to that, since

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the device can be turned on at zero current early enough before the current pulse is fired. Second, it is clear that any pulse, however short, induces a certain amount of device self-heating; the knowledge of the junction thermal time constant is thus essential to determine the error resulting from a pulse of given length, possibly also allowing for a compensation procedure.

The characterization curves presented in Section 3.3 suggest important guidelines for the in-circuit characterization of on-state resistance as TSEP. Comparing the two curves related to the thermal chamber in Figure 16 (green for short pulses, red for longer ones), it is clear that the junction self-heating is a problem in this kind of tests. The red trace is obtained with millisecond-long pulses: this is "long" for laboratory purposes, but compatible with the bandwidth of typical current control loops used in power converters, especially when highly inductive loads are used. To overcome this limitation, pulses with a duration lower than 100 µs should be used, possibly requiring a dummy load (different from the actual one) and a high-bandwidth current loop. If pulses longer than the junction thermal time constant are used, an error ranging from 8 % to 16 % can arise (see Figure 16), thus degrading the accuracy of the whole TSEP characterization.

The superposition of the green, blue and magenta curves in Figure 16 suggests that the "fast" thermal chamber and Kapton characterization procedures are equivalent; comparing the blue and magenta curves (Kapton-embedded resistor heating, TSEP read using an external load or the CST, respectively) it is interesting to notice that the method used to create the current pulse is almost irrelevant, while heating the device from its case is functionally equivalent to doing it from the ambient. This can be partly justified considering that in the thermal chamber the device is not mounted on the heat sink, while it is in the Kapton case. In both cases, most of the heat flows through the most thermally conductive part of the device body, i.e., its metal back.

The CST curve (black) in Figure 16, instead, follows a different path, especially at higher temperatures. This can be ascribed to the different way in which the device is heated: using CST, the heat flows from the inner part of the device to the outside; combining this with the large thermal capacity of the heat sink and the non-ideal thermal connection of the NTC sensor (placed on the top of the device package, see R_{js} and R_{sa} in Figure 10) delays reaching thermal equilibrium, resulting in the black curve diverging from the others above 50 °C.

Figure 17 gives a slightly different picture: heating with the Kapton film and measuring using CST (magenta) still gives accuracy comparable with the thermal chamber (green); heating and sensing with the Kapton film (i.e., letting the measuring current flow on an external load) (blue) seems to disrupt the procedure. However, in principle there are no reasons for the two curves to be apart, which leads us to believe that there could have been an issue in the RTD resistance measurement in the two experimental runs. This is reasonable, since the base value for the RTD varied of several ppm at the beginning of each test, and even if zeroing procedures have been carried out, an error could still be present. In fact, the overall RTD variation over the whole observed temperature span is just 0.86 % (60 °C · 144 ppm/K). On the other hand, the CST curve is much more consistent with the "cold" thermal chamber case, revealing a better thermal connection between the junction and the Kapton embedded RTD than with the NTC thermistor. Regardless of the way in which the device temperature is determined, it is clear how the in-place characterization procedure must rely on a narrower temperature span: differently from the thermal chamber, the device is mounted on an effective heat sink, designed for the real converter application, which efficiently dissipates heat to the ambient, thus limiting the maximum temperature achievable during the characterization procedure. However, the fitting function interpolating the experimental points can be used to extrapolate the $R_{ds,on}$ value at higher temperature values.

In addition to the practical information about the on-state resistance as a TSEP discussed above, Section 3.4 gives a prominent result about TSEPs in general. Since the $R_{ds,on}$ is constant in that experiment, the DUT temperature is not changing; the change in the CST

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current is caused by the CD, which is heating up under an important shoot-through power loss. Since the gate driver used is capable of generating a single V_{st} value, the change in CST current is solely a consequence of the change in the threshold voltage of the CD, due to its varying (increasing) temperature. Thus, it is clear that the CST current at constant gate voltage is another TSEP which, differently from on-state voltage, does not require any clamping circuit to be measured: it can be read directly on the current sensors that are commonly already available in the circuit for control purposes, provided that their bandwidth is large enough. This recalls past works about the saturation current of IGBTs as TSEP, such as [17]; the main difference here is that the technique allows the measurement without with the need of a load or of any assumption about its nature.

5. Conclusions

This work has demonstrated the possibility to calibrate TSEP curves for the MOSFET on-state resistance out of the laboratory and in the field. Namely, we have explored two procedures that can be used in-place (or in-circuit), with the power device mounted in its circuit. The CST-based procedure, already presented in [8], has been carefully compared with state-of-the-art thermal chamber curves, paying special attention to the duration of the current pulse used for the measurement and to the artifacts connected to the limited bandwidth of the clamping circuit.

Moreover, we introduced a novel technique based on a resistive element, working both as heater and sensor, embedded in Kapton films, yielding performance comparable to the thermal chamber procedure and outperforming the CST method, even though the temperature range that can be effectively explored during the procedure, requiring thermal equilibrium between the case and its junction, is narrower than that achieved in the chamber (this is unavoidable, since power devices are almost always mounted on heat sinks in real-world working environments). It is also interesting to note that the curves obtained in the chamber, with the device detached from the circuit, and those with the device in-circuit, are almost overlapping, which shows that the thermal coupling via TIM and heat sink does not alter the TSEP characteristics.

Despite its relative ease of mount, the Kapton embedded RTD is difficult to read, because of sub-optimal resistance values (optimized for heating) and poor sensitivity. The hardware-linearized NTC, despite its inherent thermal resistance when mounted on the device top, presents itself as a much viable and inexpensive option, if conditioned using the proposed approach. In addition, a novel TSEP which can be measured in-place with ease has been discovered: the CST current. Its use could remove the need for a clamping circuit to measure the on-state voltage, but the full potential of this new TSEP will be explored in future works, while adapting the present characterization procedure to it.

In conclusion, if an in-place characterization procedure is sought, RTDs embedded in thermally conductive films used as TIMs for attaching the device to the heat sink are a viable option, provided that an additional temperature sensor is available or a high-sensitivity resistance measurement is adopted. CST can profitably be used to create very short current pulses, suitable for measuring the on-state resistance while avoiding self-heating. Nonetheless, CST heating, due to the different heat flow path in the converter assembly, requires long times to reach thermal equilibrium on the sensors, thus presenting poor accuracy at higher temperatures.

Author Contributions: Conceptualization, A.S. and R.M.; methodology, A.S.; software, A.S. and M.D.; validation, all; formal analysis, A.S. and R.M.; investigation, A.S. and M.D.; resources, R.M.; data curation, M.D.; writing—original draft preparation, A.S. and C.C.; writing—review and editing, R.M. and C.C.; visualization, M.D.; supervision, A.S.; project administration, R.M.; funding acquisition, R.M. and A.S. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

AGD	Active Gate Driver
CD	Complementary Device
CST	Controlled Shoot-Through
DUT	Device Under Test
LDC	Loss Distribution Coefficient
NTC	Negative Temperature Coefficient (thermistor)
PTC	Positive Temperature Coefficient
RTD	Resistance Temperature Detectors
SNR	Signal-to-Noise Ratio
SOA	Safe Operating Area
TC	Thermocouple
TCR	Temperature Coefficient of Resistance
TIM	Thermal Interface Material
TSEP	Temperature-Sensitive Electric Parameter
VCCS	Voltage-Controlled Current Source

Appendix A. List of symbols

i_d drain current in linear region [A]

$i_{d,sat}$ drain current in saturation region [A]

v_{gs} gate-source MOSFET voltage [V]

v_{ds} drain-source MOSFET voltage [V]

$v_{ds,on}$ on-state drain-source MOSFET voltage [V]

$R_{ds,on}$ on-state drain-source resistance [Ω]

V_T MOSFET threshold voltage [V]

β large-signal MOSFET gain [A/V^2]

P_{max} maximum power to be dissipated [W]

r loss distribution coefficient [1]

R_T NTC thermistor resistance [Ω]

R_0 NTC thermistor nominal resistance at ambient temperature (25 °C) [Ω]

R_F Film resistance [Ω]

R_{F0} Film resistance at 0 °C [Ω]

α TCR of film resistance [1/°C]

V_{dc} DC voltage at half bridge input [V]

P_{st} CST-induced power loss [W]

I_{st} CST current [A]

t_{st} CST pulse duration [s]

c CSTduty cycle [1]

T_{sw} switching period [s]

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