Article

Novel Dead-time Compensation Strategy for wide current range in a three-phase inverter

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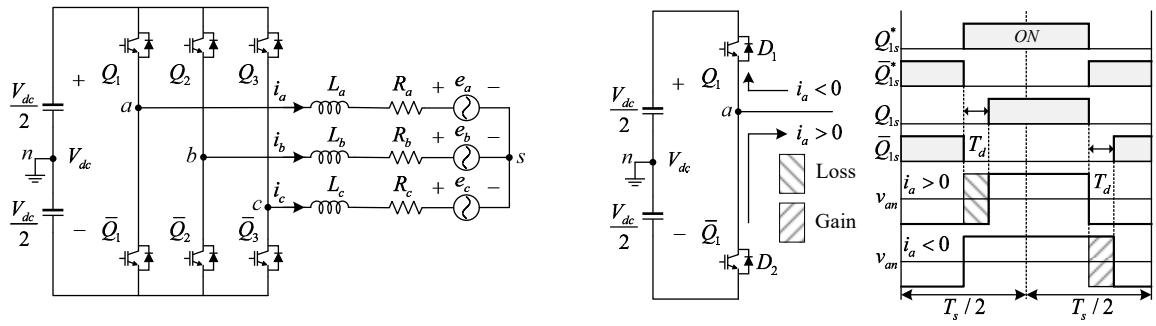
Abstract: This paper proposes a novel three - phase voltage source inverter dead-time compensation strategy for accurate compensation in wide current regions of the inverter. In particular, an analysis of the output voltage distortion of the inverter, which appears as parasitic components of the switches, has been conducted for proper voltage compensation in the low current region, and an on-line compensation voltage controller has been proposed. Also, a new trapezoidal compensation voltage implementation method using the current phase is proposed to simplify realizing the trapezoidal shape of the three-phase compensation voltages. Finally, when the proposed dead-time compensation strategy is applied, the maximum phase voltage magnitude in the linear modulation voltage regions is defined to achieve smooth operation even at high modulation index. Simulations and experiments were conducted to verify the performance of the proposed dead-time compensation scheme.

Keywords: DTCS; dead-time compensation; trapezoidal compensation voltage; dead-time effects; three-phase VSI compensation

1. Introduction

The dead-time is an efficient strategy which is adding blank time within complementary switching signals to prevent arm-short. The series two switches circuit sharing a DC-link such a half-bridge, is activated complementarily to keep arm-short condition. However, in the actual switch, a delay occurs within on/off operating due to the parasitic components, the series switches appear to be shorted with a DC-link. The short circuit allows excessive current through the series switches, causing serious system failure. Therefore, the reliability of the system can be guaranteed by injecting enough dead-time T_d until the switch reaches a steady state [1-2], [5-17].



(**a**) (**b**)

Figure 1. three-phase VSI and dead-time switching patterns in a-phase: (a) typical three-phase VSI configuration; (b) switching patterns and output voltages of the half-bridge during the dead-time.

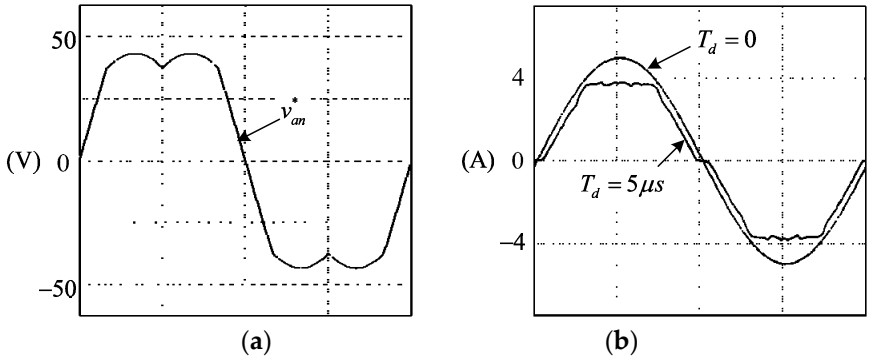


Figure 2. Effects of the dead-time in three-phase VSI (f_{sw} =20kHz, V_{dc} =100V, L_s =0.01mH, R_s =10Ω); (a) an a-phase pole voltage reference with SVPWM; (b) comparing dead-time effects with equal voltage reference at Figure 2 (a).

Especially, as shown in Figure 1 (a), a circuit structure such as a typical three-phase VSI in which three legs share a DC-link must ensure a reliability of the system by applying dead-time. Figure 1 (b) shows the process of the leg in a-phase according to time during the single switching period. $Q^*_{1s}, \bar{Q}^*_{1s}$ are ideal complementary switches on/off signals and $Q_{1s}, \bar{Q}_{1s}$ are real switch on/off signals adapted the dead-time T_d. Since the dead-time can't control actively, it causes not only serious voltage distortions in inverter output voltage as shown Figure 1 (b) but also adverse effects on the all algorithms using a voltage reference, thereby generating an error voltage between the real inverter output voltage and the voltage reference [3-4]. The Figure 2 (a) demonstrates a pole voltage reference and (b) illustrates current waveforms with Figure 2 (a) to confirm the current distortions by dead-time. Here, when the dead-time is applied, it can be recognized that the critical current distortion occurs near the zero crossing points and peak area.

Various types of dead-time compensation strategies have been published to analyze and compensate for the dead-time defects. In [1-2], [5], the dead-time and the switch on/off delay are analyzed and suggest dead-time compensation method via theorical parameters. However, since the switch parameters are fluctuated with external factors, it is difficult to compensate accurately in all inverter operating areas by using fixed variables. In some papers [6-8], the distortions of inverter output voltage by switch's output capacitors studied and suggested compensation strategies with the look-up table containing the switch-off times according to the magnitude of the current. Although, it has a disadvantage that is difficult to compensate the precise dead-time in various environments since the table is limited to the experimental environment. The papers [9-10] proposed on-line dead-time compensation voltage (DTCV) modification methods that feeds back current distortions. However, the strategies extracting of the current errors are complicate and it has the drawbacks near the zero-crossing points. In [11], the dead-time compensation algorithm using filter has been suggested. Nevertheless, due to the lowpass-filter characteristics, the bandwidth of the current controller can be limited. The paper [12], it submits scheme which is compensates the sixth-order harmonic in d-q axis currents on the synchronous reference frame using bandpass filter. But, the performance of the dead-time compensation scheme is limited by the current controller performance because of the distortion errors input to the current reference. The [13-14] offer compensation strategies using observer which is feeding back d-q axis currents on synchronous reference frame. However, the observer regards not only the dead-time distortions but also various parasitic components as dead-time errors, since it is utilizing an ideal-model. Thus, it is impossible to accurately estimate the real output voltage of inverter. In [15-16], the on-line dead-time compensation algorithms having the trapezoidal shape compensation voltage and the modulator for slope have been proposed. However, it is difficult to completely compensate for the non-linearities of the switch especially low current region.

In this paper, a novel DTCS is proposed for correct dead-time compensation and for normal operating in wide-current region. In section 2, the inverter output voltage error is analyzed by the

dead-time and the switch's non-linearities. In section 3, it presents the proposed novel DTCV implementation strategy to revise the shape of the TCV and the on-line TCV controller. In section 4, the three-phase VSI distorted output voltage due to the dead-time is analyzed on the space vector and the maximum linear-modulation phase voltage (MMPV) is also done when the proposed DTCS is applied. Finally, in section 5, the simulation and the experiment are implemented to verify the proposed DTCS. And the performance of the DTCS is evaluated with phase current total harmonic distortion (THD).

2. Analysis of dead-time effects

In this paper, the dead-time T_d of (2) is including the ON/OFF propagation delay in order to simply express as V_d. And the conduction voltage drops across the diode and switch are excluded from the effect of dead-time because they are negligible compared to the dc-link voltage level.

2.1. The three-phase VSI output voltage errors by the dead-time

In figure 1 (b), the inverter output voltage v_{an} is varied according to the phase current i_a direction during the dead-time. When the current direction is in the positive, the current flows through the body diode D_2 in the lower switch $\bar{Q}_1$, so that the v_{an} come to be $-V_{dc}/2$. On the other hand, when the current direction is in the negative direction, the current flows though the body diode D_1 in the upper switch Q_1, thus the output v_{an} becomes $V_{dc}/2$. Therefore, the a-phase pole voltage errors due to the dead-time can be expressed as

$$\Delta v_{an}^{err} = \begin{cases} -V_d & (i_a > 0) \\ V_d & (i_a < 0) \end{cases} \tag{1}$$

$$V_d = \frac{T_{on} + T_d - T_{off}}{T_s} V_{dc} \tag{2}$$

In equation (2), the V_d is average pole voltage error (APVE) that occurs during single switching period, and it contains switch turn on/off delays T_{on}, T_{off} as well as dead-time T_d [2]. The a-phase APVE can be expressed according to the direction of current as shown equation (1), also the other phases b, c can be expressed in the same approach via each current polarity [1]. The APVEs of three-phase are represented by the voltage errors on the synchronous reference frame d-q axis as follows.

$$\begin{bmatrix} \Delta v_{as}^{err} \\ \Delta v_{bs}^{err} \\ \Delta v_{cs}^{err} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} \Delta v_{an}^{err} \\ \Delta v_{bn}^{err} \\ \Delta v_{cn}^{err} \end{bmatrix} \tag{3}$$

$$\begin{aligned} \begin{bmatrix} \Delta v_d^{err} \\ \Delta v_q^{err} \end{bmatrix} &= \begin{bmatrix} \cos\theta_e & \sin\theta_e \\ -\sin\theta_e & \cos\theta_e \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} \Delta v_{as}^{err} \\ \Delta v_{bs}^{err} \\ \Delta v_{cs}^{err} \end{bmatrix} \\ &= -\frac{4V_d}{\pi} \begin{bmatrix} -\sin\delta - \sum_{n=1}^{\infty} \left\{ \frac{\sin(6n\omega_e t - \delta)}{(6n-1)} + \frac{\sin(6n\omega_e t + \delta)}{(6n+1)} \right\} \\ \cos\delta - \sum_{n=1}^{\infty} \left\{ \frac{\cos(6n\omega_e t - \delta)}{(6n-1)} - \frac{\cos(6n\omega_e t + \delta)}{(6n+1)} \right\} \end{bmatrix} \end{aligned} \tag{4}$$

The equation (3) indicates average phase voltage errors by transferring the three-phase APVEs and equation (4) denotes the average d-q axis voltage errors on synchronous reference frame by the Fourier series expansion [5] [11]. Where the δ is the phase angle between the q-axis and the three-phase current vector I_s as shown Figure 3.

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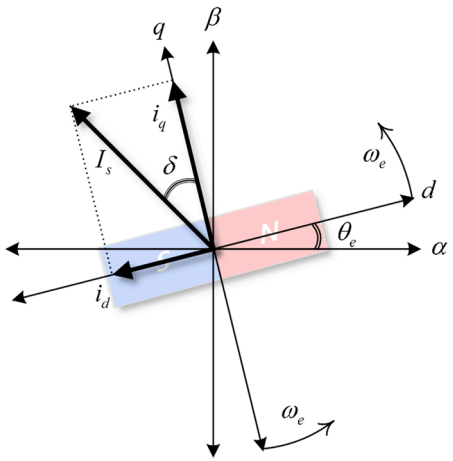


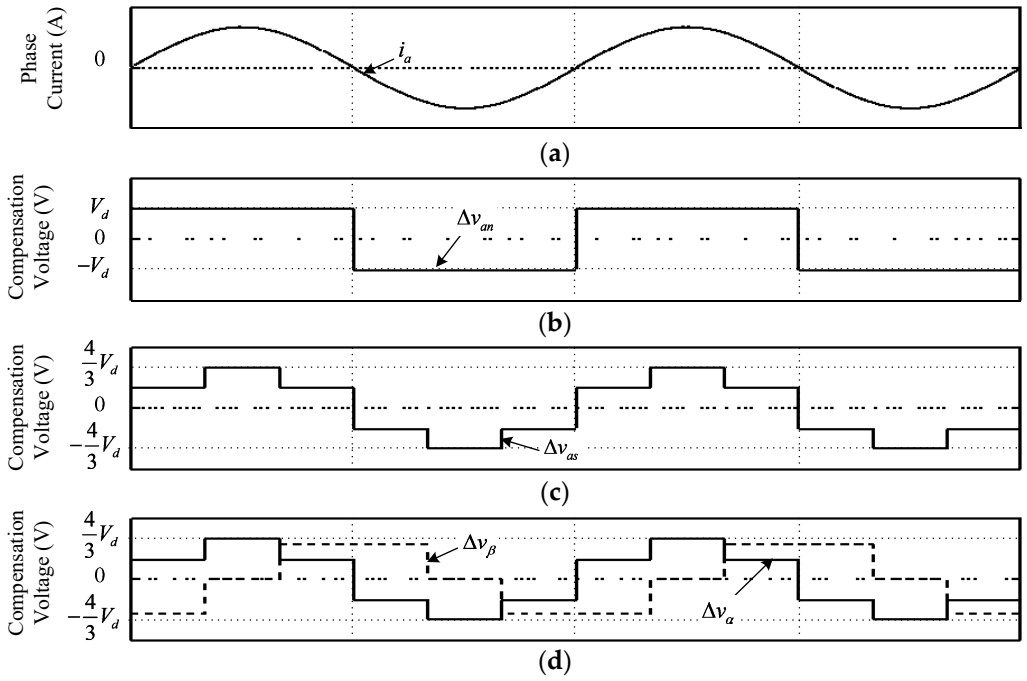
Figure 3. Stationary reference frame $\alpha-\beta$ axis and synchronous reference frame $d-q$ axis with δ.

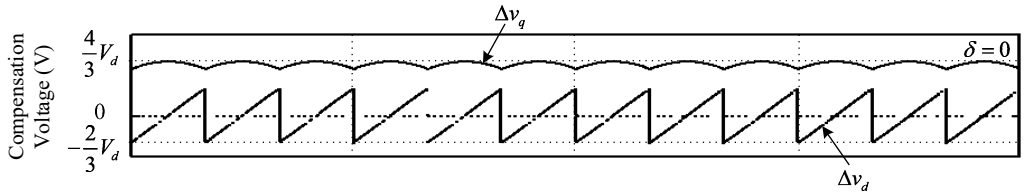
The d-q axis voltage error contains both the fundamental and $6n^{\text{th}}$ harmonics distortion as equation (4). Theses voltage errors cause discordance between the real output voltage of three-phase VSI and the voltage references. Furthermore, the distortion components causing harmonic currents which degrades the performance of the VSI. Therefore, in order to compensate the voltage distortions due to the dead-time, the opposite voltage of the error voltage can be applied through the equation (1). The average compensation pole voltage (ACPV) can be expressed as follows.

$$\Delta v_{an} = V_d \text{sign}(i_a) \tag{5}$$

$$\text{sign}(i_a) = \begin{cases} 1 & (i_a > 0) \\ -1 & (i_a < 0) \end{cases} \tag{6}$$

The ACPVs of b, c -phases can be describe in similar way as equations (5), (6) which is a-phase AVPC [1-2]. Using the ACPVs of three-phase with synchronous reference frame transformer in equation (5), (6), the d-q axis compensation voltage waveforms can be illustrated as Figure 4.



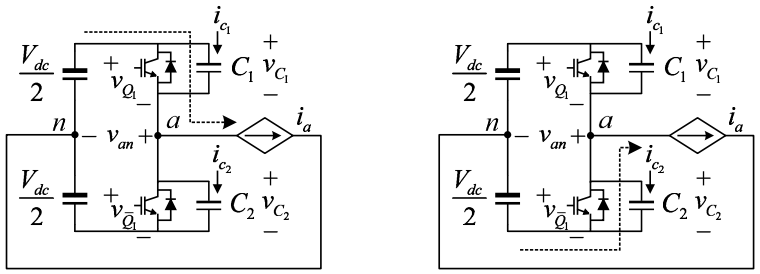


(e)

Figure 4. Dead-time compensation voltage waveforms; (a) a-phase current; (b) ACPV of a-phase; (c) the average compensation phase voltage of a-phase; (d) compensation voltages on stationary reference frame $\alpha - \beta$ axis; (e) compensation voltages on synchronous reference frame $d - q$ axis;

2.2. The effects of swtich's parasitic components

The switch contains diverse parasitic components and the output capacitor of the switch is critical factor in compensating the distorted output voltage of three-phase VSI because of it seriously affects the switch off delay time T_{off} depending on the magnitude of the phase current [6]. Figure 5 shows the output capacitors C_1, C_2 connected in parallel with the switches and the charging and discharging process when the phase current i_a flows in the positive direction.



(a) (b)

Figure 5. Charging and discharging process of the output capacitors $(i_a > 0)$.

In Figure 5 (a), the voltage $(v_{C_1} = V_{dc})$ charged in capacitor C_1 is discharged while the upper switch is turn on. At the moment, the discharging current $-i_{C_1}$ flows to the node 'a' due to the potential difference and charges the capacitor C_2 of the lower switch. Since the impedance between the capacitor C_1 and C_2 is very small than the load, most of the current $-i_{C_1}$ flows to the capacitor C_2, so that the voltage v_{C_2} of the lower switch parasitic capacitor C_2 is rapidly charged to V_{dc}. Consequently, when the upper switch is turned on, the output pole voltage v_{an} of the inverter is hardly affected. On the contrary, when the both upper and lower switches are turned off as shown in Figure 5 (b), the capacitor C_2 of the lower switch is discharged and the voltage of v_{C_2} arrives at zero. At this time, the phase current i_a can be expressed by the sum of the charge current i_{C_1} of the upper switch and the discharge current i_{C_2} of the lower switch.

$$i_a = -i_{C_2} + i_{C_1} \tag{7}$$

Assuming that the capacitances C_1, C_2 and the charging/discharging potentials are equal, the time T_{off} required for discharging v_{C_2} can be formulated as follows.

$$C_1 = C_2 = C_{12} \tag{8}$$

$$\left|i_{C_2}\right| = \left|i_{C_1}\right| = \frac{\left|i_a\right|}{2} \tag{9}$$

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$$v_{C_2}\left(T_{off}\right)=\frac{1}{C_{12}}\int_0^{T_{off}}-i_{C_2}(t)dt+v_{C_2}(0) \tag{10}$$

From the equation (11), if the initial value is V_{dc}, the following equations (11), (12) can be obtained.

$$-V_{dc}=\frac{1}{C_{12}}\int_0^{T_{off}}-\frac{|i_a|}{2}dt \tag{11}$$

$$\therefore T_{off}=\frac{2C_{12}V_{dc}}{|i_a|} \tag{12}$$

If the phase current i_a flows in the opposite direction, the switch delay occurs in the upper switch in a similar way when the current flowing in the positive direction as shown Figure 5. Thus, the upper switch turns off delay time is the same as in equation (12) [17]. The Figure 6 shows a graph comparing the time T_{off}^{eq} calculated by equation (12) and the time T_{off}^{sim} measured by simulation result in Figure 5. It can be confirmed that the switch turns off delay time changes non-linearly along with the magnitude of the phase current. Therefore, to accurately compensate the distorted three-phase VSI output voltage, it is necessary to compensate for the appropriate switch delay according to the current magnitude because the influence of T_{off} is remarkable in the low current region.

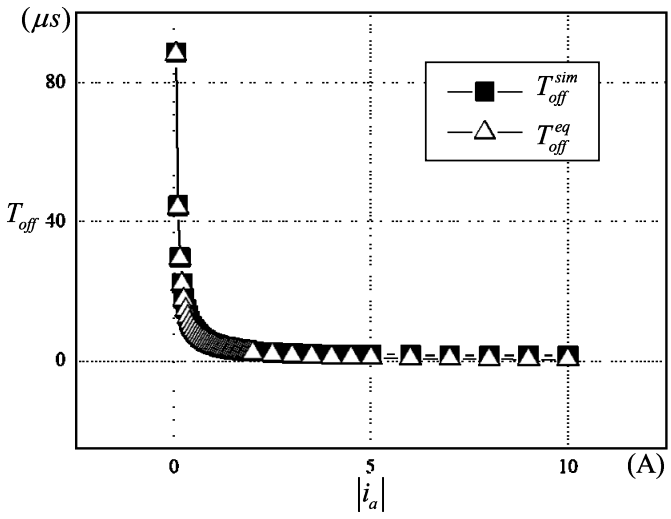
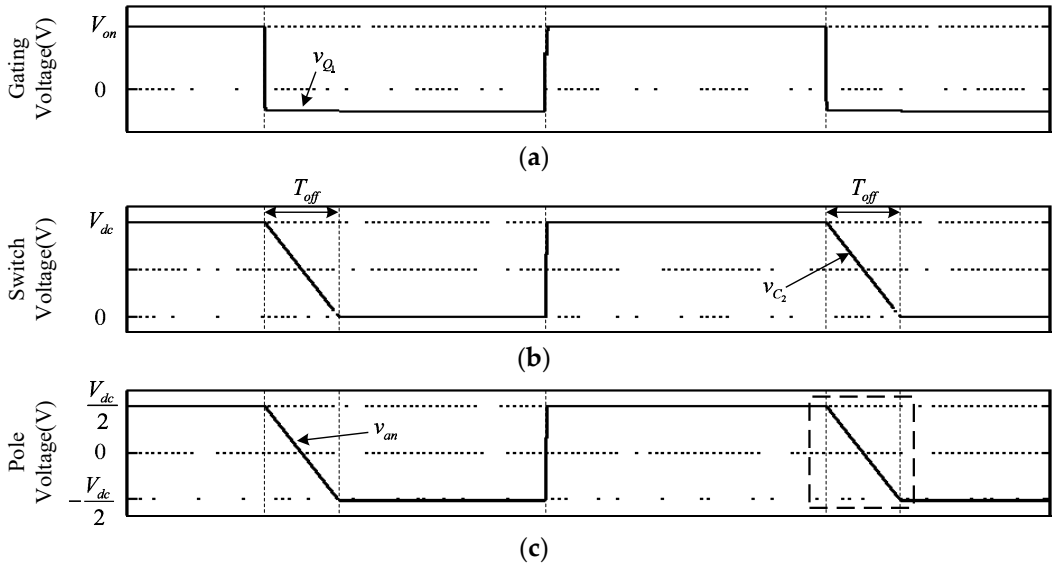


Figure 6. Comparing with T_{off}^{eq} and T_{off}^{sim}.

The Figure 7 shows the simulation results of the circuit Figure 5. the symbols v_{Q_1}, v_{C_2} are meaning the gate voltage of the upper switch, the voltage of the lower switch respectively and the v_{an} is output pole voltage. When the phase current i_a is positive direction, the output pole voltage of the VSI represented as

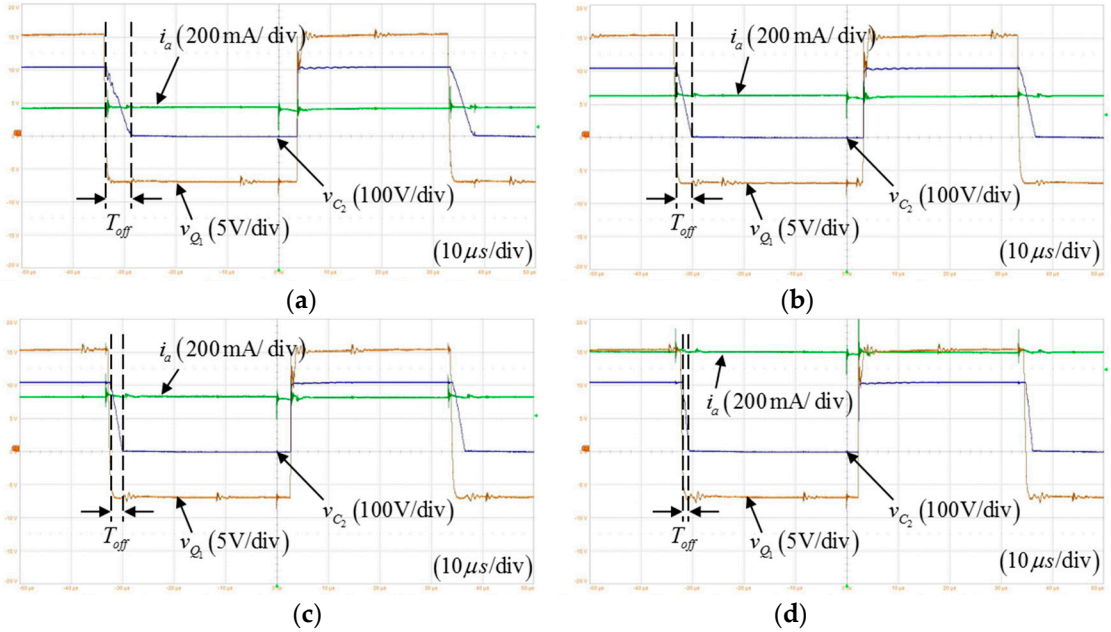
$$v_{an}=-\frac{V_{dc}}{2}+v_{C_2} \tag{13}$$

In here, the v_{C_2} affects the output of the VSI since it is discharged with a slope depending on the amplitude of $|i_a|$ as shown in Figure 7. Therefore, the v_{C_2} should be properly compensated because of it can't be actively controlled.



152 **Figure 7.** Simulation results of Figure 5 $\left(T_{off} < T_d\right)$; (a) gate voltage v_{Q_1} ; (b) capacitor voltage v_{C_2} of
153 the lower switch; (c) inverter pole voltage v_{an} .

154 The Figure 8 shows the waveforms of real switch and the phase currents to compare with Figure
155 7 which is simulation results.



156 **Figure 8.** Variation of the T_{off} according to the phase current magnitude; (a) i_a =170mA; (b) i_a
157 =250mA; (c) i_a =330mA; (d) i_a =600mA.

158 The equation (2) is applicable when the current level is enough to saturate the T_{off} and the
159 voltage of the capacitor is rapidly falling or rising. Therefore, the output pole voltage changes the
160 polarity with substantially constant slop as Figure 9, since the low current region where the effects of
161 the turn off delay is maximized as Figure 7, 8. Consequently, it is necessary to redefine the
162 compensation voltage considering the slop of the output capacitor voltage.

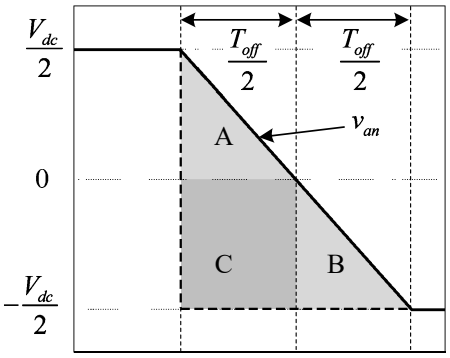


Figure 9. Detail of the dashed box in Figure 5 (c).

The regions A, B and C are non-controllable voltages caused by the output capacitors in Figure 9 and it requires appropriate voltage compensation for the ideal inverter output. The voltage region Δv_{C_2} made by the output capacitor can be described as

$$\Delta v_{C_2} = \mathrm{A} - (\mathrm{B} + \mathrm{C}) \tag{14}$$

If each area is defined as equation (15), (16) and (17), the parasitic voltage region Δv_{C_2} represented as equation (18)

$$\mathrm{A} = \frac{1}{2}\left(\frac{V_{dc}}{2}\frac{T_{off}}{2T_s}\right) \tag{15}$$

$$\mathrm{B} = \frac{1}{2}\left(-\frac{V_{dc}}{2}\frac{T_{off}}{2T_s}\right) \tag{16}$$

$$\mathrm{C} = -\frac{V_{dc}}{2}\frac{T_{off}}{2T_s} \tag{17}$$

$$\Delta v_{C_2} = \frac{T_{off}}{2T_s}V_{dc} \tag{18}$$

Equation (2) can be redefined as equation (19), in order to properly compensate the output capacitor in the low current region in which the switch turns off delay has the greatest effect on the three-phase VSI.

$$\therefore V_d = \frac{T_{on} + T_d - \frac{T_{off}}{2}}{T_s}V_{dc} \tag{19}$$

3. The proposed DTCS

As mentioned above, the voltage error not only caused by dead-time distortion but also caused by switch parasitic are should be compensated to obtain the ideal three-phase VSI output. In the equation (19), the generally dead-time T_d is fixed value, but the delay time T_{off} is not. Hence, the precise T_{off} has to be calculated according to the phase current levels in real-time for correct compensation. In this paper, the TCV is used to simplify the variation of T_{off} [8], [15]. In addition, the novel implementation strategy is proposed to simplify the realizing trapezoidal shape voltage, also the novel on-line TCV controller is proposed to robust for variating parameters.

3.1. The implementaion of the TCV based on the current position

The proposed DTCS uses synchronous reference frame transformation matrix and limiter function to simplify realizing the TCV. Figure 10 shows the triangle waveform function $f(t)$, the sinusoidal waveform function $g(t)$ with peak value k and the trapezoidal waveforms utilizing them to comparing the outline. In Figure 3, the position of the three-phase current θ_d can be calculated as follows using the d-q axis currents.

$$\delta = \tan^{-1}\left(\frac{i_d}{i_q}\right) \tag{20}$$

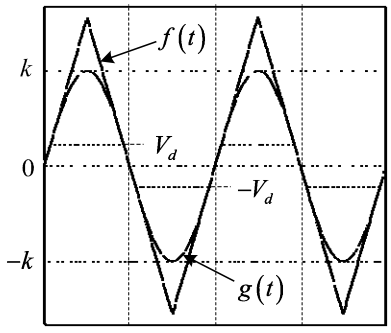
$$\theta_d = (\theta_e - \delta) \tag{21}$$

The three-phase sinusoidal waveforms, which is in phase with the three-phase current vector I_s, can be defined as follows. $\alpha-\beta$ axis voltage $g(\Delta v_\alpha), g(\Delta v_\beta)$ with peak value k on the stationary reference frame expressed as

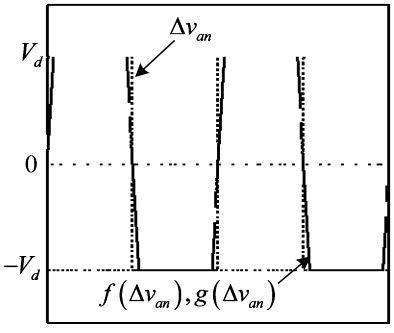
$$\begin{aligned} g(\Delta v_\alpha) &= -k\sin\theta_d \\ g(\Delta v_\beta) &= k\cos\theta_d \end{aligned} \tag{22}$$

$g(\Delta v_\alpha), g(\Delta v_\beta)$ is transferred to a three-phase stationary coordinate and the amplitude is limited to $\pm V_d$ as equation (23) to generate the TCV as shown in Figure 10 (b).

$$\begin{cases} g(\Delta v_{an}) = g(\Delta v_\alpha) & (-V_d \le g(\Delta v_{an}) \le V_d) \\ g(\Delta v_{bn}) = -\dfrac{\left(g(\Delta v_\alpha) - \sqrt{3}g(\Delta v_\beta)\right)}{2} & (-V_d \le g(\Delta v_{bn}) \le V_d) \\ g(\Delta v_{cn}) = -\dfrac{\left(g(\Delta v_\alpha) + \sqrt{3}g(\Delta v_\beta)\right)}{2} & (-V_d \le g(\Delta v_{cn}) \le V_d) \end{cases} \tag{23}$$



(a)



(b)

Figure 10. Proposed implementation strategy for TCV; (a) triangle waveform function $f(t)$ and sinusoidal waveform function $g(t)$ with peak k; (b) TCV comparison made by $f(t)$ with $g(t)$.

As can be seen in the Figure 10 (b), if the peak level k is large enough to approximate a linear slope between V_d and $-V_d$, then the waveforms can be reckoned as $f(\Delta v_{an}) \approx g(\Delta v_{an})$. Next, as illustrated in Figure 11, the peak value k for implementing the TCV having slopes of the width ϕ can be defined as follows.

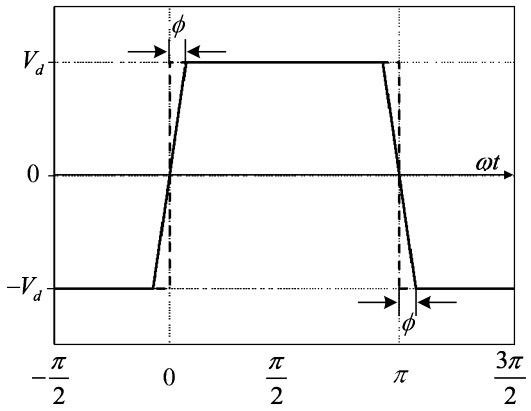


Figure 11. TCV with slopes of the width ϕ.

The function $g(t)$ can be express as $g(t) = k\sin(\omega t)$, and the time when $g(t)$ has a slopes of the width ϕ defines as t_ϕ, then the time t_ϕ can be derived as

$$t_\phi = \frac{\phi}{\omega} \tag{24}$$

Assuming that the output of $g(t)$ is $|V_d|$ at the time t_ϕ, the $g(t)$ rewritten as

$$k\sin(\omega t_\phi) = |V_d| \tag{25}$$

Therefore, the peak value k of the function $g(t)$ obtaining slope of the width ϕ is defined as equation (26)

$$\therefore k = \frac{|V_d|}{\sin(\phi)} \tag{26}$$

The adjustable TCV having a desired compensation voltage amplitude $|V_d|$ and compensation voltage slope of width ϕ can be realized with equations (23) to (26).

3.2. The on-line TCV controller

It can be seen from Figure 6 and equation (19) that the proportions of APVE must be varied according to the amount of the current flowing in the phase. Especially, when the VSI operates in the low current region, the magnitude of the APVE and the slopes of the TCV are decreased. For this reason, for smooth dead-time compensation in wide current regions, both the scale of the APVE and the slope of the TCV must be modulated to optimum value corresponding to the inverter operating environment.

Using the previously defined equations (12), (19) and (26), it is possible to vary the amplitude of APVE by responding to T_{off}. However, there is limitations to actively react changing conditions.

Therefore, a controller using the errors of the TCV is proposed to implement robust dead-time compensation even unknown operating conditions.

While the influence of the dead-time appears $6n^{\text{th}}$ harmonics in the synchronous reference frame as equation (4), the TCV errors can be generated using them [16]. The extracting axis can be selected as a d-axis although the $6n^{\text{th}}$ harmonics appear on both d-q axis, since the d-axis has larger voltage error than q-axis has. But if there is a d-axis current ($\delta \neq 0$), the fundamental component of the distortion voltage is shared with q-axis shown in equation (4). Thus, to obtain a constant value regardless of amount of d-axis current, the synchronous reference frame based the three-phase current vector I_s should be carried out. In this, if the d-axis current for TCV error attained from the equation (20), (21), the harmonics do not emerge on d-axis since the harmonic components of the current affects the phase δ . For this reason, the ideal phase of three-phase current vector I_s can be gotten by the d-q axis current references i_d^*, i_q^* as following equation (27), (28), assuming that the actual currents do not deviate for the current commands.

$$\delta^* = \tan^{-1}\left(\frac{i_d^*}{i_q^*}\right) \tag{27}$$

$$\theta_d^* = \left(\theta_e - \delta^*\right) \tag{28}$$

The controller error i_{dd} is calculated from the d-q axis transfer matrix in equation (4) and the phase of ideal three-phase current vector I_s (28).

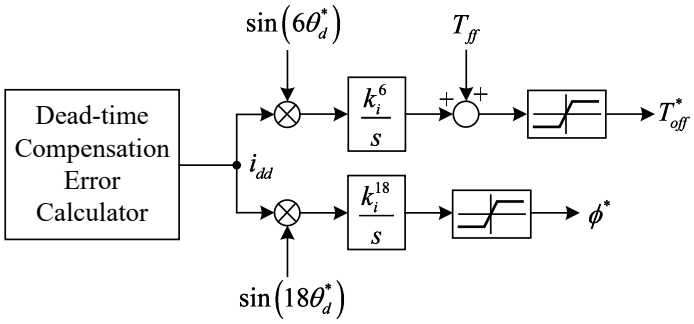
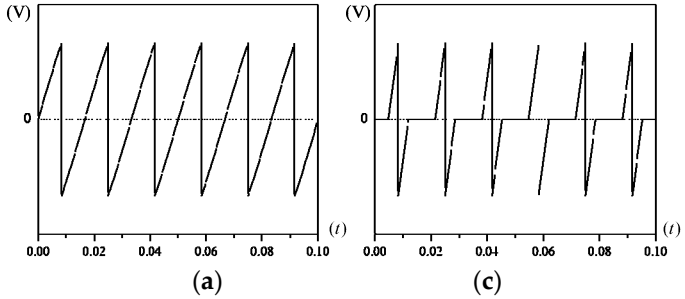


Figure 12. The proposed on-line TCV controller.

The d-axis current i_{dd} based on θ_d^* includes the current distortion of the $6n^{\text{th}}$ harmonics as per influence of the TCV errors, and the polarity of them can be determined by multiplying each order harmonic via θ_d^* [16]. Figure 12 demonstrates the proposed on-line TCV controller. To adjust the turn off delay time and slope of the TCV, the integrators are designed and for faster dynamics, T_{ff} from the equation (12) is feedforwarded. While the T_{off}^* is a factor controlling the maximum APVE, the phase current i_s in equation (12) must be altered as the three-phsae currents amplitude I_s .



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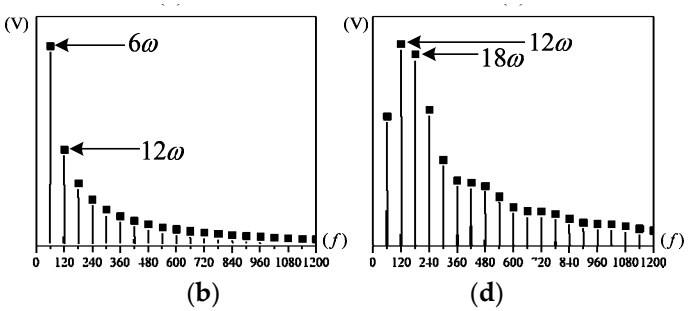


Figure 13. Analysis of DTCV error characteristics on the synchronous reference frame; (a) error voltage of V_d; (b) FFT result of Figure 13 (a); (c) error voltage of slop of DTCV; (d) FFT result of Figure 13 (c).

Figure 13 indicates the fast fourier transform (FFT) results for two types of the DTCV errors. Figure 13 (a) shows the voltage waveform of the V_d error. And the FFT result of the V_d error has prominent component in the 6th harmonic as Figure 13 (b). Figure 13 (c) demonstrates the voltage waveform of the slope error. And the FFT result of the slope error has noticeable element in the 12th and 18th harmonics as Figure 13 (d).

By utilizing the results of the Figure 13, the 6th harmonic and 18th harmonic can be selected as error factors of the T_{off} and the ϕ respectively such as Figure 12. The 18th harmonic is picked as a slope error to minimize the influence of the 6th harmonic instead of the 12th.

4. The analysis of the linear modulation region with proposed DTCS

The proposed DTCS the way feedforwarding the DTCV at the controller output which voltage references. Thus, when the correct DTCV is applied, the dead-time effect does not come out at the controller sides. However, if the controller outputs a voltage command exceeding the inverter output limitation, the feedforwarding compensation voltage will not be able to suitable compensate due to physical constraints of the hardware. Therefore, it is required to limit the voltage reference of the controller by applying the proper physical voltage limit to the controller in order to perform normal operating of the DTCS.

4.1. The defination of the MMPV of the three-phase VSI

Table 1. The phase voltages and space voltage vectors of the three-phase VSI.

Vector	Phase voltage			Space voltage vector
	v_{as}	v_{bs}	v_{cs}	
V_1^i	$\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}/0^\circ$
V_2^i	$\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	$\frac{2}{3}V_{dc}/60^\circ$
V_3^i	$-\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}/120^\circ$
V_3^i	$-\frac{2}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}/180^\circ$
V_5^i	$-\frac{1}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	$\frac{2}{3}V_{dc}/240^\circ$
V_6^i	$\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}/300^\circ$

O	0	0	0	0 / 0°

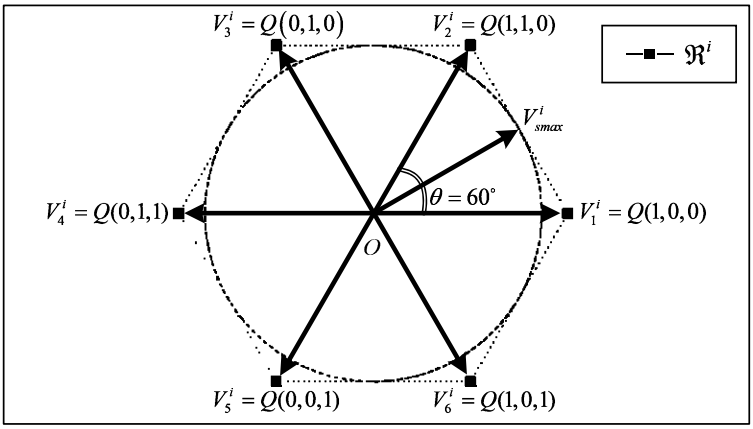


Figure 14. Six output voltage vectors of typical three-phase VSI.

Table 1 and Figure 14 are express the voltage vectors of the three-phase VSI in Figure 1. The hexagonal region $\Re^i$ using the six active voltage vectors is ideal voltage area. The switching operation state function $Q(Q_n, Q_n, Q_n)$ of each leg in Figure 14 is shown as

$$Q(Q_1,Q_2,Q_3)\begin{cases} Q_n = 1: & Q_n = on, \overline{Q}_n = off \\ Q_n = 0: & \overline{Q}_n = on, Q_n = off \end{cases} \tag{29}$$

In Figure 14, V_{smax}^i is the magnitude of the MMPV in the region $\Re^i$. When arbitrary voltage reference V^* presents at $0^\circ \le \theta \le 60^\circ$, it can be configured during the switching period T_s with the neighboring active voltage vector V_1^i, V_2^i and zero voltage vector O.

$$\int_0^{T_s} V^* dt = \int_0^{T_1} V_1^i dt + \int_{T_1}^{T_1+T_2} V_2^i dt + \int_{T_1+T_2}^{T_s} O dt \tag{30}$$

Where T_1, T_2 represent the interval for which the vectors V_1^i, V_2^i is applied, respectively. The maximum active voltage vector with V_1^i, V_2^i is

$$V^* T_s = V_1^i T_1 + V_2^i T_2 \tag{31}$$

The reference vector V^* projected on the V_1^i and V_2^i vectors, respectively, can be given as

$$V_1^i T_1 = V^* T_s \cos\theta - V_2^i T_2 \cos 60^\circ \tag{32}$$

$$V_2^i T_s = V^* T_s \frac{\sin\theta}{\cos 30^\circ} \tag{33}$$

The periods of each voltage vector T_1, T_2 can be obtained with equation (32), (33)

$$T_1 = \gamma T_s \cos\theta - \frac{\gamma T_s}{\sqrt{3}} \sin\theta \quad \left(where \quad \gamma = \frac{3}{2}\frac{V^*}{V_{dc}} \right) \tag{34}$$

$$T_2 = \frac{2\gamma T_s}{\sqrt{3}} \sin\theta \tag{35}$$

Here, since $T_1 + T_2 \le T_s$, equations (34), (35) can be derived as equation (36)

$$V^* \left(\cos\theta + \frac{1}{\sqrt{3}} \sin\theta \right) \le \frac{2}{3} V_{dc} \tag{36}$$

$$V^* \le \frac{V_{dc}}{\sqrt{3}} \frac{1}{\sin(\theta + 60^\circ)} \tag{37}$$

$$\therefore V_{smax}^i = \frac{V_{dc}}{\sqrt{3}} \quad (where \quad \theta = 30^\circ) \tag{38}$$

Accordingly, the MMPV amplitude V_{smax}^i at $\theta = 30^\circ$ in the ideal three-phase VSI can be defined as equation (38)

4.2. The analysis of the linear modulation region with dead-time and proposed DTCS

The distortion voltage that occurs in dead-time can be derived by using equations (3) to (6) and be demonstrated distorted voltage region with Figure 14. In this case, the affection of the distorted voltage caused by the dead-time depends on the phase ψ of the current. Thus, the distortion voltage can be defined as the function of ψ as $\Delta v_\alpha^{err}(\psi), \Delta v_\beta^{err}(\psi)$ on the stationary reference frame $\alpha - \beta$ axis. Where the maximum three-phase VSI output with six active voltage vectors is v_α^i, v_β^i, the distorted three-phase VSI output, the v_α^r, v_β^r can be express as

$$\begin{bmatrix} v_\alpha^r \\ v_\beta^r \end{bmatrix} = \begin{bmatrix} v_\alpha^i \\ v_\beta^i \end{bmatrix} + \begin{bmatrix} \Delta v_\alpha^{err}(\psi) \\ \Delta v_\beta^{err}(\psi) \end{bmatrix} \tag{39}$$

The Figure 15 defines the phase ψ between the voltage reference and phase current.

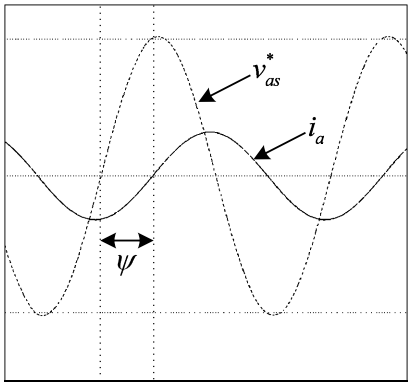


Figure 15. The current phase ψ with a-phase voltage reference v_{as}^* and a-phase current i_a.

Figure 16 illustrates the distorted three-phase VSI output voltage waveforms v_α^r, v_β^r on the stationary reference frame $\alpha - \beta$ axis according to the phase ψ. Figure 17 shows v_α^r, v_β^r regions on the x-y plot using the waveforms in Figure 16 and equation (39), and the right side of each voltage region reveals the sector ① in detail for more accurate analysis.

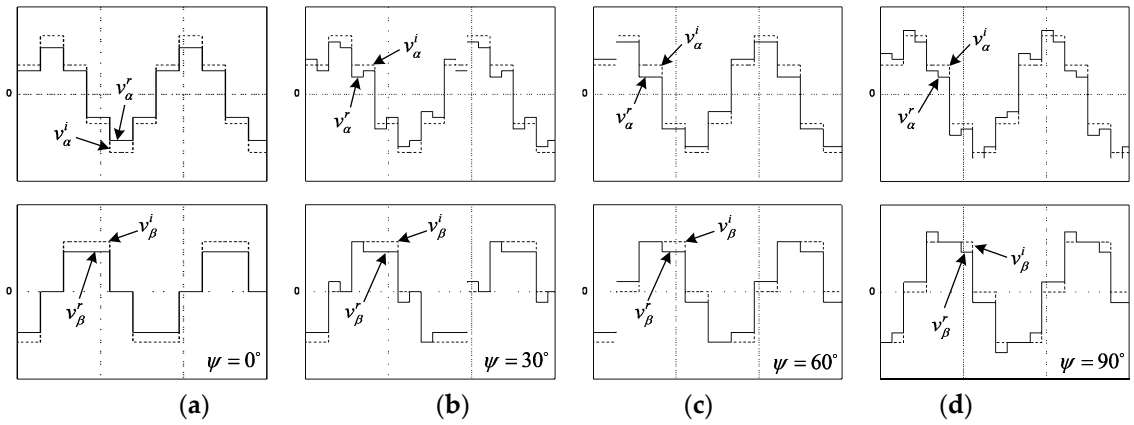
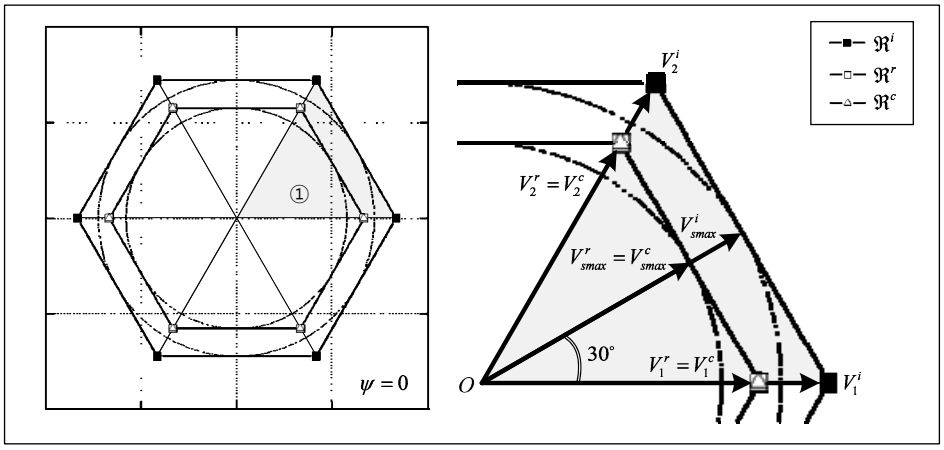


Figure 16. Voltage waveforms v_α^i, v_β^i and v_α^r, v_β^r on the stationary reference frame according to the phase ψ; (a) $\psi = 0°$; (b) $\psi = 30°$; (c) $\psi = 60°$; (d) $\psi = 90°$.



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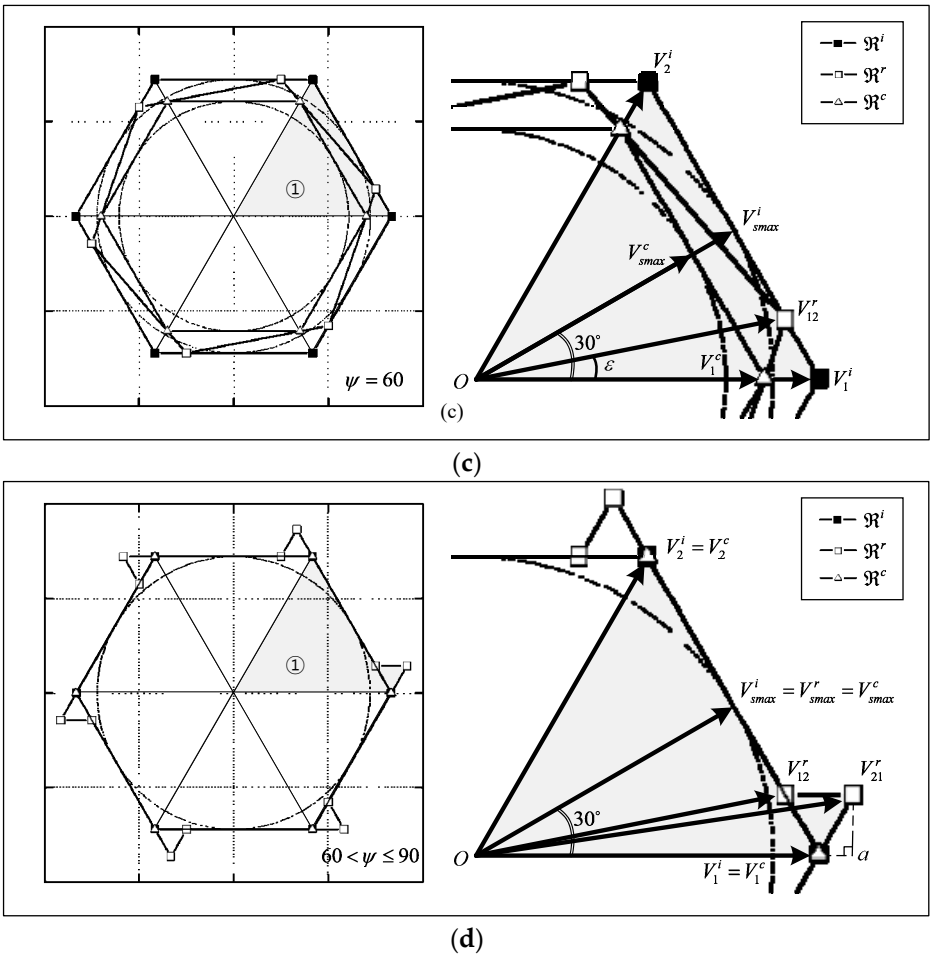

Figure 17. Distorted voltgae regions according to the current phase ψ ; (a) $\psi = 0^\circ$; (b) $0^\circ < \psi < 60^\circ$; (c) $\psi = 60^\circ$; (d) $60^\circ < \psi \le 90^\circ$.

Figure 17 (a), (b), (c) and (d) are divided into four regions along the voltage region forms. In the case of ψ being a negative phase value as a leading, it has a same form with a positive phase value as Figure 17 since the distortion voltage from the dead-time is even function. Therefore, the MMPV levels arrange in a Table 2 instead of illustrating the regions about negative phase value. Where $\Re^i$, $\Re^r$ and $\Re^c$ are the output voltage region of the ideal three-phase VSI, the output voltage of the three-phase VSI distorted by the dead-time and the output voltage region of the three-phase VSI applied proposed DTCS. Because of the dead-time physically limits the period the turn on time of the switch, even if the dead-time compensated, the physical limits of the inverter can not be recompensed. Consequently, when the proposed DTCS is applied, the compensated region $\Re^c$ is inscribed voltage region in the dead-time region $\Re^r$.

Table 2. The compensated MMPV V_{smax}^c when the proposed DTCS applied.

Phase delay of current	Phase voltage V_{smax}^c
$\psi = 0^\circ$	from (42) $\frac{V_{dc} - 2V_d}{\sqrt{3}}$
$0^\circ < \psi < 60^\circ, -60^\circ < \psi < 0^\circ$	from (43) $\frac{V_{dc} - 2V_d}{\sqrt{3}}$

$\psi = 60^\circ$, $\psi = -60^\circ$	from (46) $\frac{\sqrt{3}}{2}\left\|V_1^c\right\|$
$60^\circ < \psi \le 90^\circ$, $-90^\circ \le \psi < -60^\circ$	from (50) $\frac{V_{dc}}{\sqrt{3}}$

4.2.1. where $\psi = 0^\circ$

When the output voltage is in phase with phase current, the voltage distortion exactly coincides with the six active voltage vectors as Figure 16 (a). Hence, by using the above equation (31) to (39), the arbitrary voltage reference V^* in the sector ① can be expressed as follows using the neighboring real voltage vectors V_1^r, V_2^r.

$$\begin{aligned} \left|V_1^r\right| &= \left|V_1^c\right| = \left|V_1^i\right| - \frac{4}{3}V_d \\ \left|V_2^r\right| &= \left|V_2^c\right| = \left|V_2^i\right| - \frac{4}{3}V_d \end{aligned} \tag{40}$$

The equation (36), (38) can be derived as

$$V^*\left(\cos\theta + \frac{1}{\sqrt{3}}\sin\theta\right) \le \frac{2}{3}\left(V_{dc} - 2V_d\right) \tag{41}$$

$$\therefore V_{smax}^r = \frac{V_{dc} - 2V_d}{\sqrt{3}} \quad (where \quad \theta = 30^\circ) \tag{42}$$

While the compensated region $\Re^c$ is equal to the distorted real region $\Re^r$, the compensated MMPV V_{smax}^c is defined as

$$\therefore V_{smax}^r = V_{smax}^c = \frac{V_{dc} - 2V_d}{\sqrt{3}} \quad (where \quad \theta = 30^\circ) \tag{43}$$

4.2.2. where $0^\circ < \psi < 60^\circ$

The proportions of the voltage vectors in Figure 17 (b) through Figure 16 (b) can be expressed as

$$V_{12}^r = \frac{2}{3}(V_{dc} - V_d) + j\frac{2}{3\sqrt{3}}V_d \tag{44}$$

$$\left|V_1^r\right| = \left|V_1^c\right| = \frac{2}{3}\left(V_{dc} - 2V_d\right) \tag{45}$$

Since the distorted real voltage vector V_{12}^r does not affect to the active voltage vector and output voltage region in Figure 17 (b), the V_{smax}^c can be derived as

$$\therefore V_{smax}^r = V_{smax}^c = \frac{V_{dc} - 2V_d}{\sqrt{3}} \quad (where \quad \theta = 30^\circ) \tag{46}$$

4.2.3. where $\psi = 60^\circ$

In Figure 17 (c), the distorted voltage vector V_{12}^r affects the real output voltage region. It can be expressed as following using Figure 16 (c).

$$V_{12}^{r} = \frac{2}{3}(V_{dc} - V_d) + j\frac{2}{\sqrt{3}}V_d \tag{47}$$

And the angle ε between the V_{12}^{r} and V_1^{i} is

$$\varepsilon = \tan^{-1}\left(\frac{\frac{2}{\sqrt{3}}V_d}{\frac{2}{3}(V_{dc} - V_d)}\right) \tag{48}$$

The maximum voltage vector magnitude $|V_1^{c}|$ in the compensated voltage region $\Re^{c}$ inscribed in the real voltage region $\Re^{r}$ is derived as

$$|V_1^{c}| = \frac{2}{3}(V_{dc} - V_d) - \frac{2}{\sqrt{3}}V_d \frac{1}{\tan\left(\frac{\pi}{3} + \varepsilon\right)} \tag{49}$$

Therefore, the V_{smax}^{c} can be defined as equation (50) using the equation (36) to (38).

$$\therefore V_{smax}^{c} = \frac{\sqrt{3}}{2}|V_1^{c}| \tag{50}$$

4.2.4. where $60^{\circ} < \psi \le 90^{\circ}$

In Figure 17 (d), the voltage vectors V_{12}^{r}, V_{21}^{r} that arisen in dead-time can be expressed as follows in Figure 16 (d).

$$V_{12}^{r} = \frac{2}{3}(V_{dc} - V_d) + j\frac{2}{\sqrt{3}}V_d \tag{51}$$

$$V_{21}^{r} = \frac{2}{3}(V_{dc} + V_d) + j\frac{2}{\sqrt{3}}V_d \tag{52}$$

The degree $\angle V_{21}^{r}V_1^{c}a$ is always 60° according to the equation (53)

$$\tan^{-1}\left(\frac{2/\sqrt{3}}{2/3}\right) = 60^{\circ} \tag{53}$$

As the line $\overline{V_{12}^{r}V_{21}^{r}}$ is parallel to the voltage vector V_1^{i}, the additional voltage region $\Delta V_{12}^{r}V_{21}^{r}V_1^{i}$ generated by the dead-time always forms a regular triangle so that the voltage vector V_{12}^{r} is adjoined with ideal voltage region $\Re^{i}$. Therefore, the compensated MMPV V_{smax}^{c} has equal magnitude with ideal modulation phase voltage V_{smax}^{i}.

$$\therefore V_{smax}^{c} = V_{smax}^{i} = \frac{V_{dc}}{\sqrt{3}} \tag{54}$$

5. The results of the simulation and experiment of the proposed DTCS

The Figure 18 is a simplified block diagram of three-phase VSI controller with the proposed DTCS. Since the DTCV is feedforwarded at the controller output, there is no need to compensate for the dead-time into the current controller state. Therefore, the error between the voltage reference of the current controller and the output voltage of the three-phase VSI can be minimized, and it makes easy to design the algorithms using the voltage reference v_{dL}^{*}, v_{qL}^{*}. As mentioned above, unless the output of the current controller is appropriately limited, normal dead-time compensation is not

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possible, so the current controller output v_d^*, v_q^* should be restricted as shown in block (b) in Figure 18. Here, the voltage limit can be defined according to the phase of the current through Table 2. Where the outside of the current controller can be designed along the employed applications.

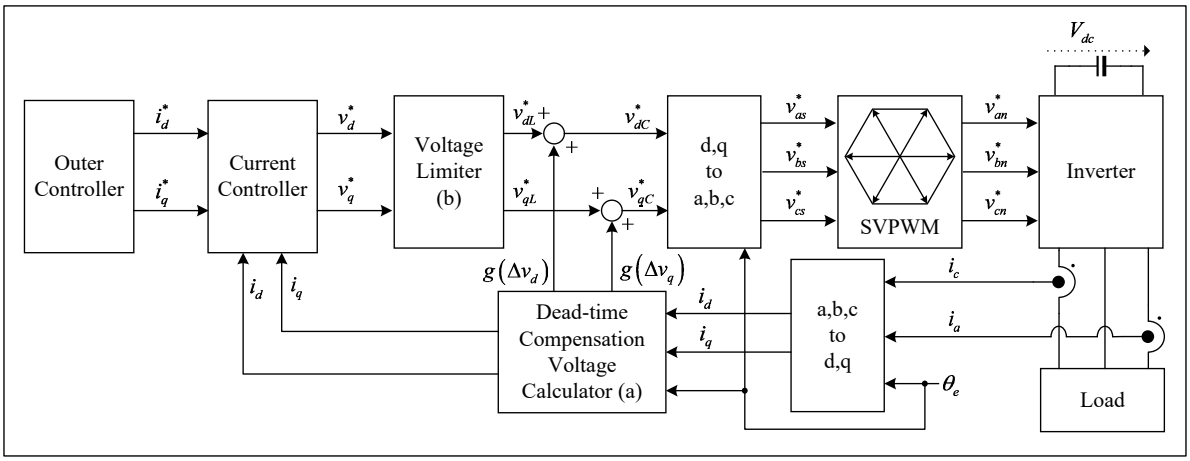


Figure 18. The control block diagram of three-phase VSI with proposed DTCS.

Figure 19 shows a block diagram of the proposed DTCS of Figure 18 (a). The TCV contains the position calculate block which calculates and outputs current angles θ_d, θ_d^* and the on-line TCV controller block which regulates ϕ, T_{off} and outputs the references ϕ^*, T_{off}^* and compensation voltage calculator block which implements TCV.

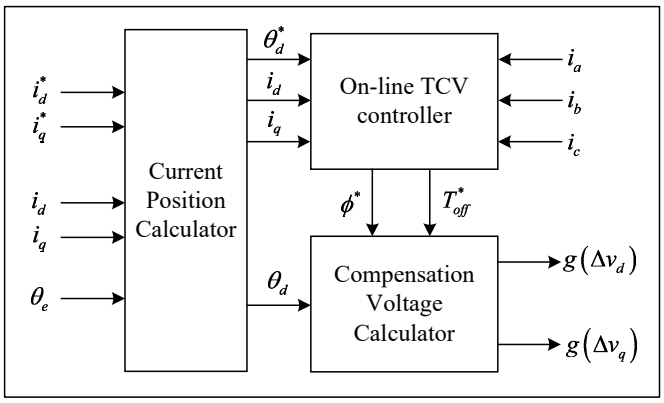


Figure 19. The specific block diagram of Figure 18 (a).

5.1. The simulation results

The proposed DTCS is verified using the simulation software Psim. The three-phase VSI and DTCS design the same as in Figure 18, and the current controller is performed alone without outer control loop. The circuit uses a three-phase VSI as shown in Figure 1. And in order to maximize the effect of dead-time, the load is composed of only the inductors and the resistors without the back electromotive force or the voltage sources. The switches modeled in SKM50GB063D manufactured SEMIKRON are used to observe the effects of the output capacitors into the simulation result. Detailed simulation specifications are shown in Table 3.

Table 3. The specifications of simulation.

Parameters	Description	Value	Parameters	Description	Value

V_{dc}	Dc-link voltage level	100 V	V_{ce}	Maximum collector - emitter voltage rating	600 V
R_s	Phase Resistance	0.5 Ω	$v_{G_{th}}$	Gate Threshold voltage	4.5 V
L_s	Phase inductance	10 mH	t_f	Fall time of the current when IGBT is turn off	300 ns
f_{sw}	Switching Frequency	20 kHz	C_{ies}	Input capacitance	2.2 nF
T_d	Dead-time	5.0 μs	C_{oes}	Output capacitance	2.2 nF
f_m	Fundamental frequency	50 Hz	R_{ce_on}	On resistance	28 mΩ

Figure 20 demonstrates the simulation results of the proposed DTCV with the above specifications. Figure 20 (a) shows the compensated 3-phsae current waveforms and (d) is the compensation voltage on the synchronous reference frame d-q axis. It can be confirmed that the magnitudes of compensation voltages $g(\Delta v_d)$, $g(\Delta v_q)$ change according to the amplitude of the current I_s and the fundamental component of the dead-time distortions shifts to the d-axis along the d-axis current magnitude. Figure 20 (e) presents the position information of the three-phase current vector I_s using the control position θ_e and equation (21). It can validate that the position of the I_s is changed along the d-q axis currents amounts.

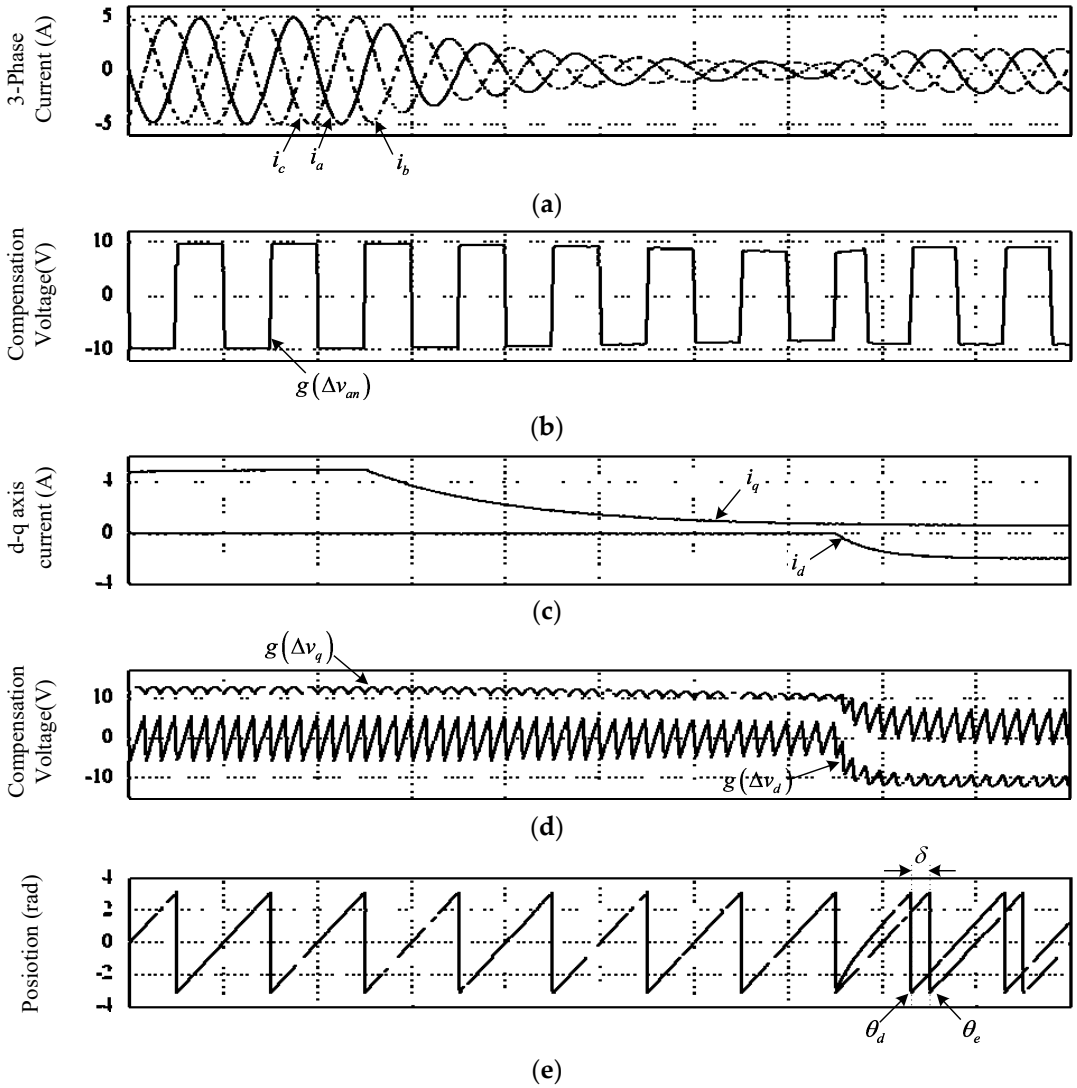


Figure 20. Simulation results of the proposed DTCS; (a) 3-phsae currents; (b) TCV of a-phase; (c) d-q axis currents on the synchronous reference frame; (d) DTCV on the synchronous reference frame d-q axis; (e) positions.

Figure 21 indicates the simulation result to comparing the performance of the proposed DTCS when any DTCS is not applied under the condition of Figure 20. Figure 21 (a) is the three-phase currents and (b) is the d-q axis current on the synchronous reference frame. As the amount of the current decreases, the harmonic distortions of the current become smaller. This is caused by the fact that as the switch turn off delay T_{off} increases in the low current region. However, when T_{off} is in the saturation region sufficiently, there is notable current distortions because of the current controller can not compensate the voltage distortion of high orderth harmonic distortions. As a result, the proposed DTCS applied three-phase currents has less than the 0.4% THD. Contrariwise, the three-phase currents which is not applied DTCS have a 5.4% THD that is about 10 times larger than that.

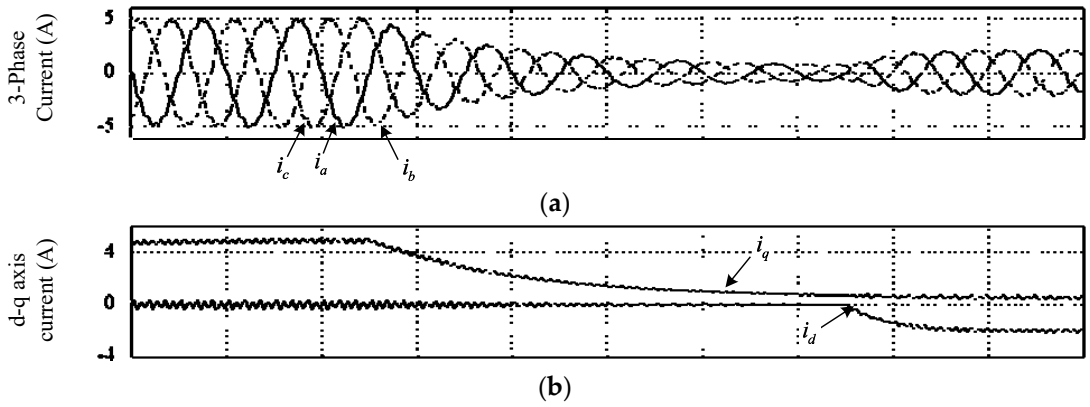


Figure 21. Simulation results without DTCS; (a) three-phase currents; (b) d-q axis currents on the synchronous reference frame.

5.2. The experimental results

The experiment to verify the proposed DTCS is used three-phase VSI connected with DC-power supply as shown Figure 22. And to maximize the effects of dead-time, it applied the only inductors and resistances as a load. Detailed stipulations of the experiment are summarized in Table 4.

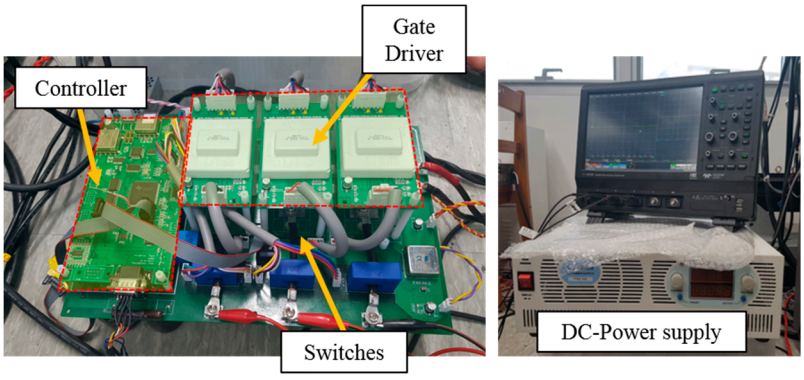


Figure 22. Experiment setting; (a) the three-phase VSI; (b) DC-power supply for the DC-link voltage source.

Table 4. Experiment specifications.

Parameters	Description	Value
Switch (Q_n)	three-phse VSI switch	SKM50GB063D

Gate driver	Gate driver of VSI	SKHI 22B
MCU	Micro controller unit	DSP 320F28335
DC Power supply	DC-link voltage source	TP5H-10D
V_{dc}	DC-link voltage level	310 V
R_s	Phase Resistance	5.5 Ω
L_s	Phase inductance	20.5 mH
f_{sw}	Switching Frequency	15 kHz
T_d	Dead-time	5.0 μs

Figure 23, 24 and 25 shows the three-phase currents waveforms for comparing the performance of the proposed DTCS with dead-time compensation pole voltage of the a-phase. The experimental conditions of the phase current were keeping about 1.4% of the switch rate to perform in the region where the effects of the switch's parasitic are present. Figure 23 is the three-phase current waveforms without DTCS, and it can be seen that serious current distortions occurs near the zero crossing. Figure 24 illustrates the three-phase current waveforms when a conventional DTCS considering only dead-time T_d is adapted. While the compensation voltage that does not reflect the variation of T_{off} is larger than the actual voltage error. It can be confirmed that the current distortion due to the excessive compensation voltage. Figure 25 reveals the currents waveforms of the proposed DTCS, which shows very sinusoidal current waveform even in the low current region where affected by T_{off} variation.

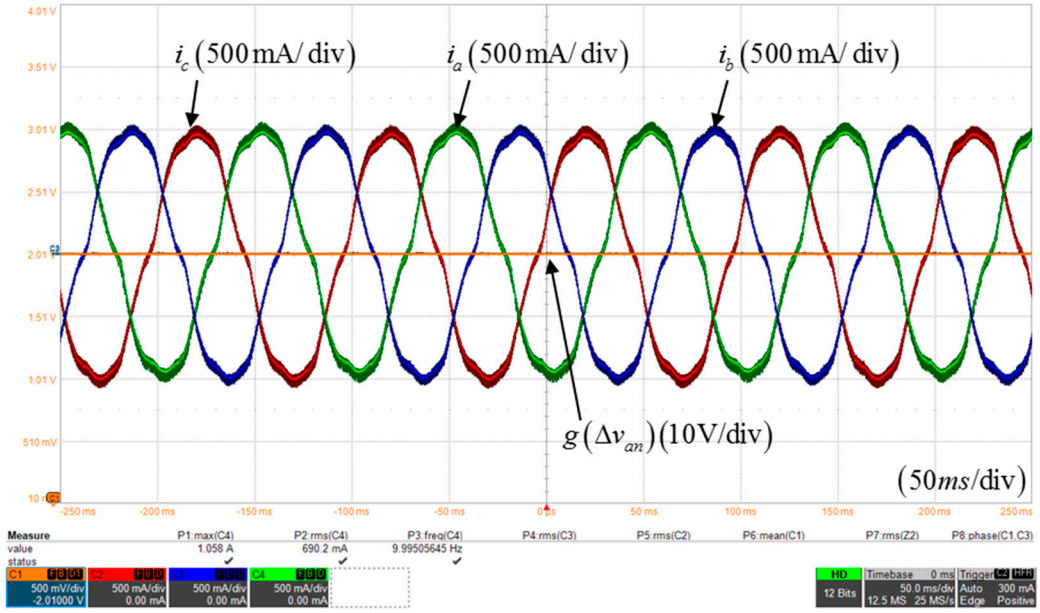
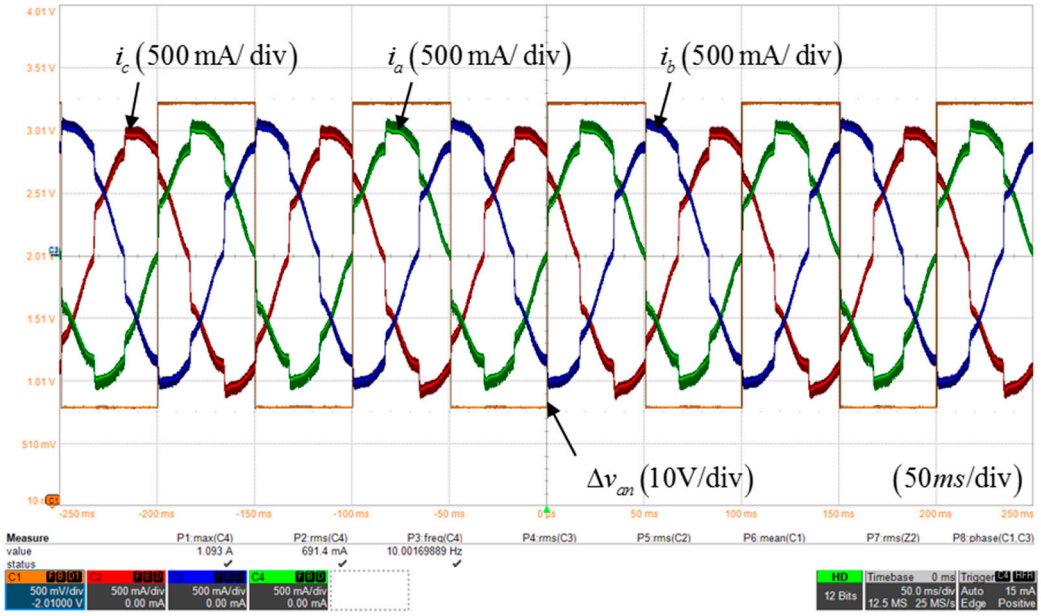
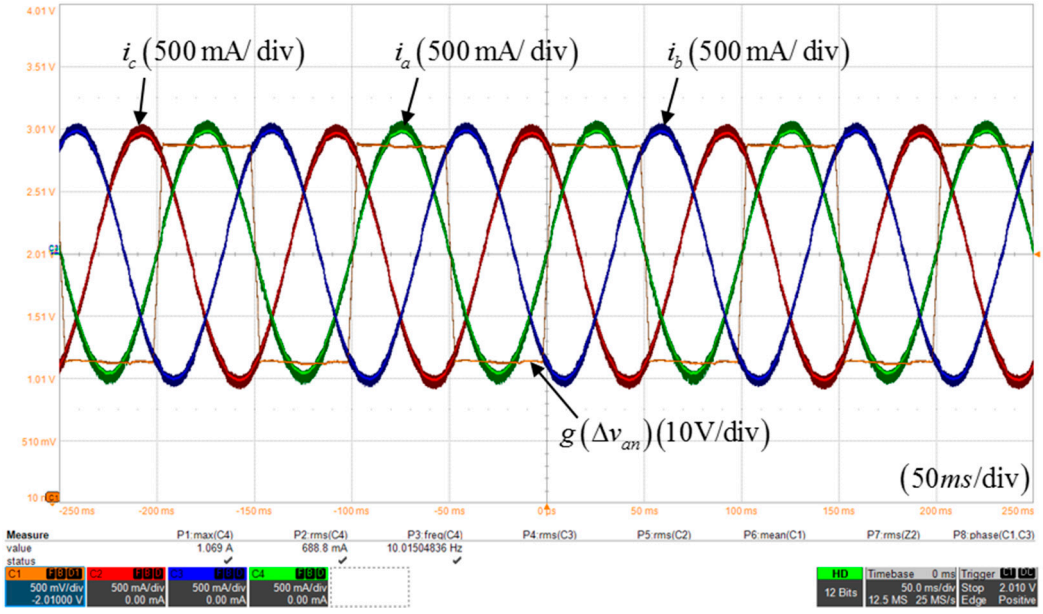


Figure 23. three-phase current waveforms with a-phase dead-time compensation pole voltage adapting dead-time.



404

405 **Figure 24.** three-phase current waveforms with a-phase dead-time compensation pole voltage in case
406 of adapting conventional DTCS.



407

408 **Figure 25.** three-phase current waveforms with a-phase dead-time compensation pole voltage in case
409 of adapting proposed DTCS.

410 The Figure 26 displays waveforms for confirming the effects of the compensating pole voltage
411 shape. The compensating pole voltage in the Figure 26 which shape is square whereas amplitude is
412 equal with Figure 25. Even if it compensated with proper voltage level, the current distortions still
413 exist near the zero-crossing points. Therefore, it can be proven that not only the amplitude of the
414 compensation pole voltage but also the slope of it is a very important factor for correct dead-time
415 compensation especially in low-current region.

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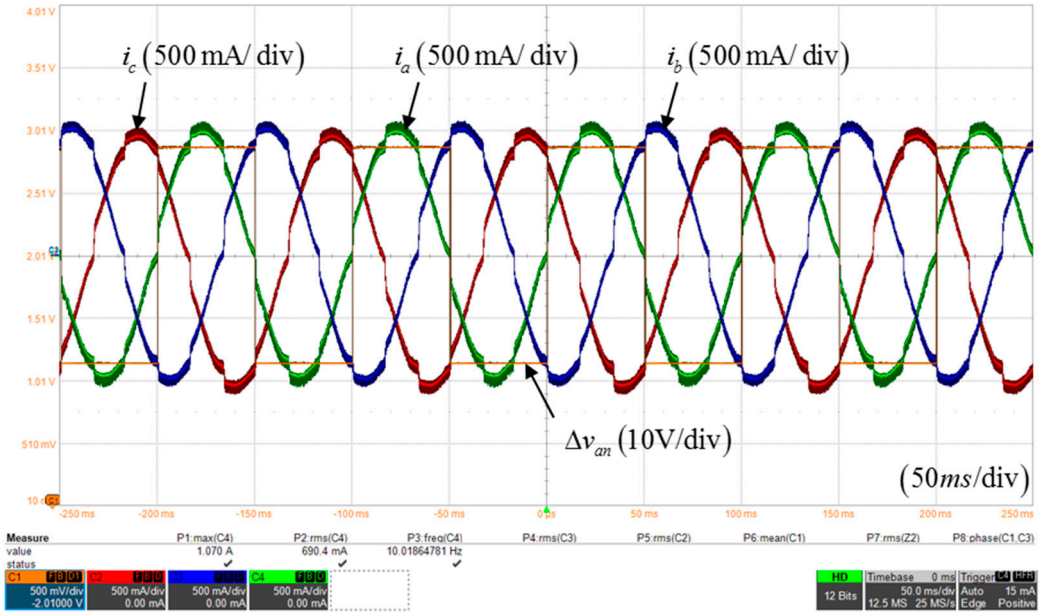

Figure 26. three-phase current waveforms with a-phase dead-time compensation pole voltage with equal amplitude with Figure 25.

The Figure 27, 28, 29 and 30 show the $\alpha-\beta$ axis currents on the stationary reference frame of above three-phase current and also demonstrate the $\alpha-\beta$ axis currents on the x-y plot that can compare the distortion of the current more intuitively. The $\alpha-\beta$ axis currents displayed using the DAC. Since α -axis current is equal the a-phase current, the both currents waveforms are overlapped to check the function of DAC. The $\alpha-\beta$ axis currents, as represented by the x-y plot, shows the ideal circular shape as the ideal sinusoidal current waveforms.

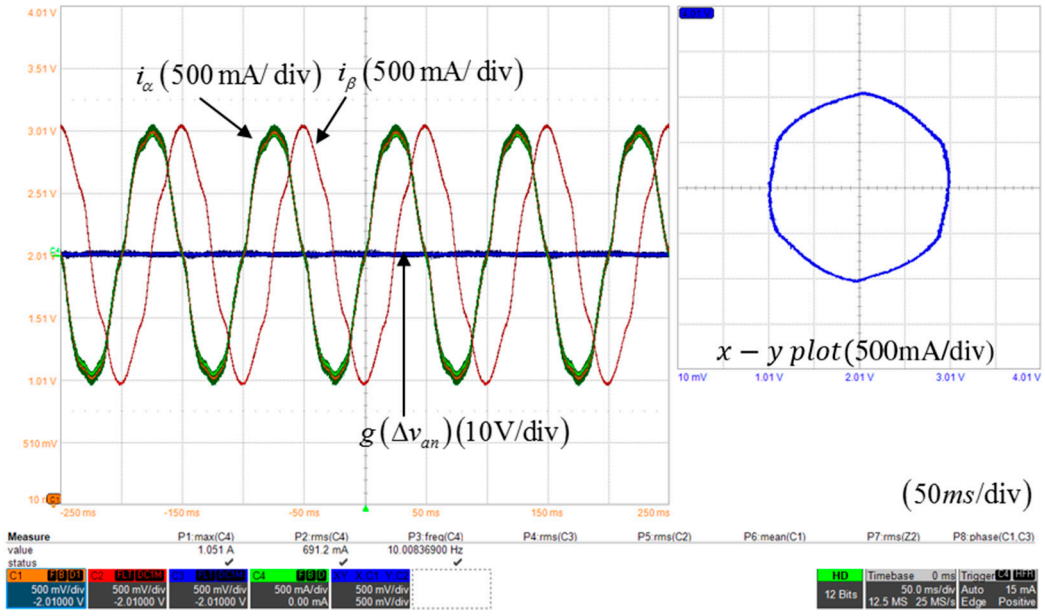

Figure 27. $\alpha-\beta$ axis currents on the stationary reference frame and on the x-y plot of Figure 23.

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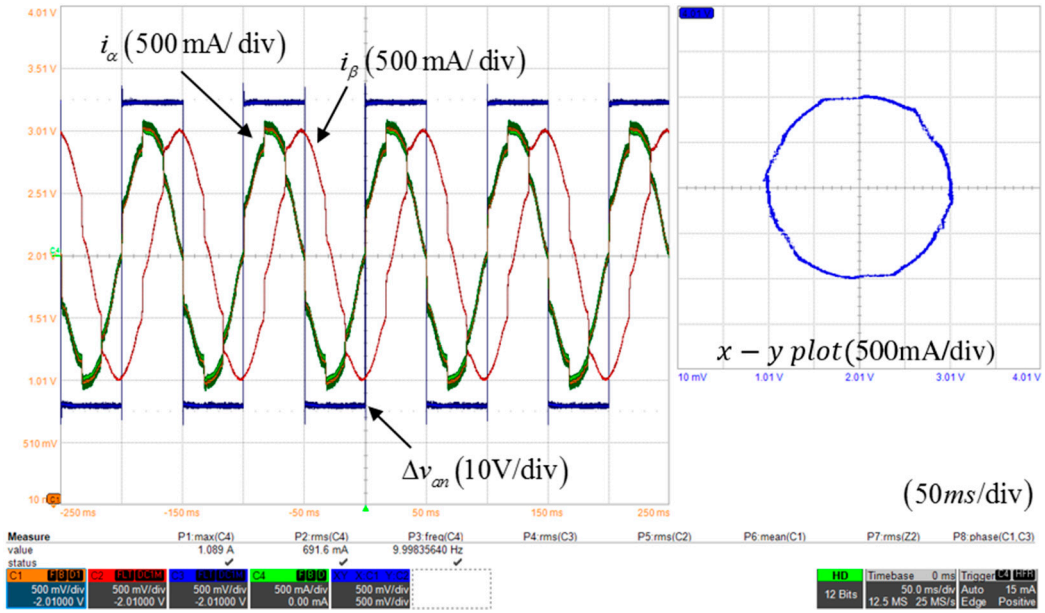

Figure 28. $\alpha-\beta$ axis currents on the stationary reference frame and on the x-y plot of Figure 24.

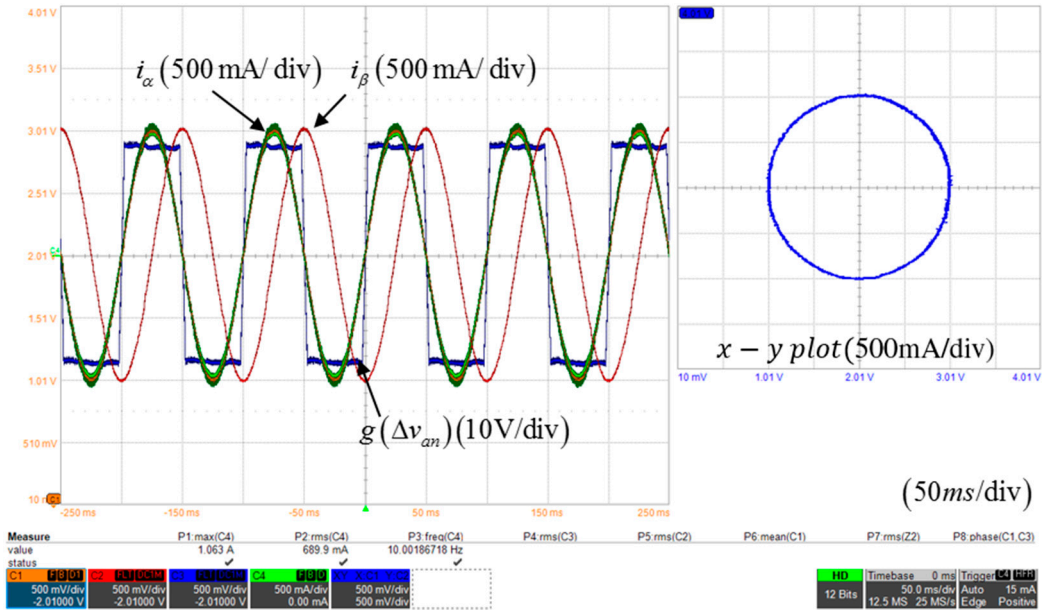

Figure 29. $\alpha-\beta$ axis currents on the stationary reference frame and on the x-y plot of Figure 25.

Figure 29 demonstrates the currents waveforms on the stationary reference frame when the suggested DTCS is applied. The currents waveform on the x-y plot is close to the ideal circle than the waveforms in Figure 26, 27. The currents waveform in Figure 30 appear closer to the circle than in the Figure 27, 38. However, due to the current distortion near the zero-crossing point, it is impossible to display the ideal circular waveform as proposed DTCS's.

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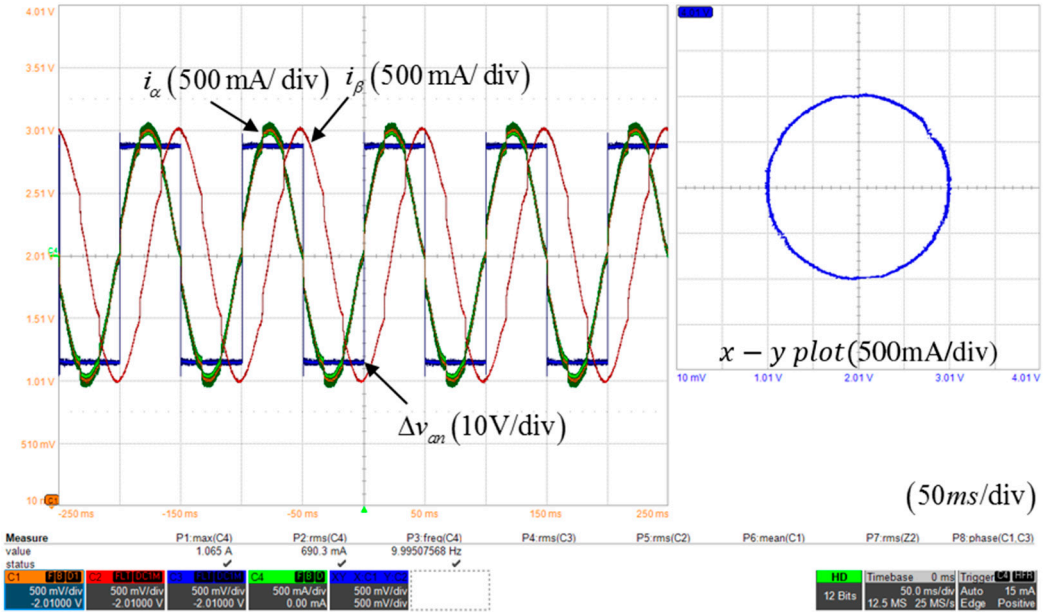

Figure 30. $\alpha-\beta$ axis currents on the stationary reference frame and on the x-y plot of Figure 26.

The current THD is computed in the several conditions to compare the performance of the proposed DTCS in Figure 31. The current THD figured according to the amplitude and fundamental frequency of the current in a-phase. The square and circle symbols represent the THD without DTCS as Figure 23 and the THD with DTCS only considering T_d as Figure 24 respectively. The triangle symbol is the THD of the a-phase current with the proposed DTCS as Figure 25. The vertical axis denotes the THD value of the a-phase current and the horizontal axis denotes the peak values of the three-phase current in Figure 31.

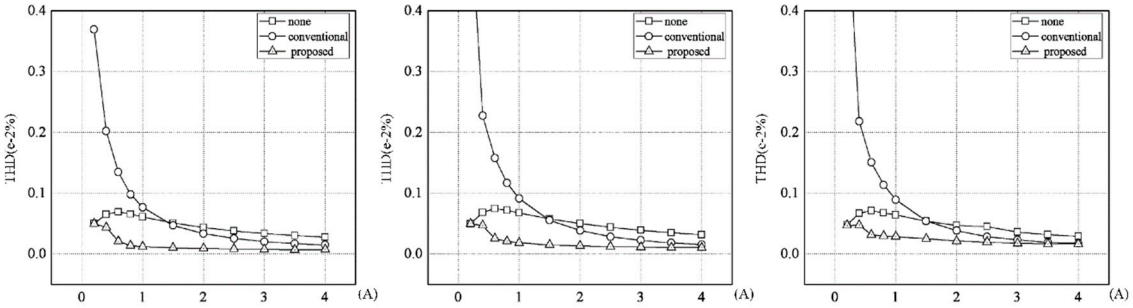

Figure 31. Comparing the THD according to the fundamental frequency of current; (a) 10Hz; (b) 30Hz; (c) 50Hz.

In case of the DTCS is applied which only considers dead-time T_d, the THD is very seriously high at the low current region where the T_{off} affects on the output voltage of the three-phase VSI. And the THD becomes decease as the current amplitude increasing because of the T_{off} effect is as saturated APVE as reduced. These results show that it is worse when inaccurate compensation voltage is applied than without any DTCS. In case of the any DTCS is not employed, the THD is low in the low current region since the influence of the dead-time is disappear due to the T_{off}. As the amplitude of the current increases, the impact of T_{off} is reduced. As a result, the current distortion gradually increases. However, the THD is becomes lower when the current level is more raised because of the duty ratio becomes enough large than the dead-time. The proposed DTSC shows much lower current THD in all current ranges. Especially, at the low current region, the proposed algorithm has a better performance than convention's by containing the on-line TCV controller.

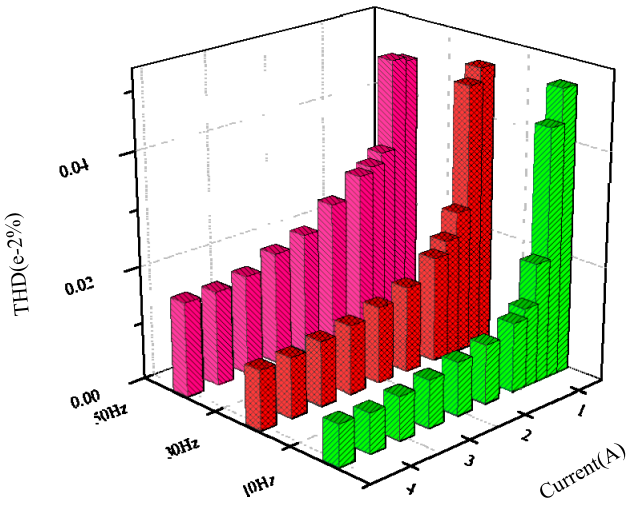

Figure 32. The differences of the THD along the fundamental frequency of the proposed DTCS.

Figure 32 shows the graphs comparing the current THD according to the fundamental frequency when the suggested DTCS is adapted. It can be realized that the current THD arises along the current frequency. The TCV should be generated to appropriate compensation but the fixed PWM is not enough to produce the slop of the TCV for the high frequency. Therefore, in the high frequency, the current THD is grown due to the imperfect TCV.

6. Conclusions

In this paper, the analysis of the output distortion of the three-phase VSI due to the dead-time and the parasitic component of the switch has been conducted, and a novel method of simply implementing the trapezoidal compensation voltage using the position of the three-phase current has been proposed. In addition, a novel compensation voltage controller is proposed to adjust the slope of the trapezoidal compensation voltage as well as the compensation voltage magnitude. That is robust to the internal parameters and current variations. An analysis of the maximum linear modulation region of the three-phase VSI is performed in parallel to normal operating at the high MI area by limiting the voltage reference. The proposed dead-time compensation strategy has been verified by simulation and experiment. The experimental results show that the it has excellent performance over all current range.

Author Contributions: J.-W.L. designed the proposed strategy and implemented the system and performed the experiments. H.Y. assisted a research and investigation process. Y.C. assisted with the idea development and paper writing.

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Conflicts of Interest: The authors declare no conflict of interest.

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