Type of the Paper (Article)

A Design of Small Area, 0.95 mW, 612–1152 MHz Open Loop Injection-Locked Frequency Multiplier for IoT Sensor Applications

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Abstract: This paper presents a 612–1152 MHz Injection Locked Frequency Multiplier (ILFM). The proposed ILFM is only used for sending an input signal to the receiver in the I/Q mismatch calibration mode. Using the Phase-Locked Loop (PLL) to calibrate the receiver places a burden on this system due to the extra area required and power consumption. Instead of the PLL, to satisfy high frequency, low jitter, and low area, a Ring Oscillator is proposed. The free-running frequency of the ILFM is automatically digitally calibrated to reflect the frequency of the injected signal from the harmonics of the reference clock. To control the frequency of the ILFM, the load current is digitally tuned with 6-bit digital control signal. The proposed ILFM locks to the target frequency using a digitally controlled Frequency Locked Loop (FLL). This chip is fabricated using 1-poly 6-metal 0.18 μm CMOS and achieve the wide tuning range of 612–1152 MHz. The power consumption is 0.95 mW from a supply voltage of 1.8 V. The measured phase noise of the ILFM is −108 dBc/Hz at a 1 MHz offset.

Keywords: injection locked frequency multiplier; Frequency Locked Loop (FLL); phase noise

1. Introduction

Recently, the Internet of Things (IoT) can be applied to many applications such as sensor networks and wearable devices. In these applications, the low power consumption and small die area are required to increase battery life and reduce system cost. Therefore, the ICs for IoT sensors should be designed to meet these requirements. The low-IF receiver architectures have become popular for low-power applications. These offer advantages over Zero-IF architecture in terms of the DC-Offset calibration and flicker noise [1]. In Low-IF architecture, the down-converted complex baseband signal is represented by two real I/Q signals. Analog parameter variations in the local oscillators, mixer and filters result in gain and phase errors between I/Q paths. Due to them, image leaks into the signal band during the down conversion process. Therefore, the low-IF receiver has the same low image rejection ratio (IRR) as shown in Figure 1 [2].

Methods for solving image problems by compensating I / Q mismatch are presented in [2]-[6]. During the I/Q mismatch calibration phase, the Injection-Locked Frequency Multiplier (ILFM) block generates the same frequency as the RF signal before receiving the RF signal through the antenna, as shown in Figure 1. Since the low-IF receiver structure crosses the I/Q signal in the band pass filter

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(BPF), the I/Q mismatch of the BPF input becomes dominant. Therefore, it is effective to add I/QMC (I/Q Mismatch Calibrator) to compensate the mismatch of I/Q signals before BPF. Figure 2 shows a block diagram of the whole low IF using ILFM and I/QMC.

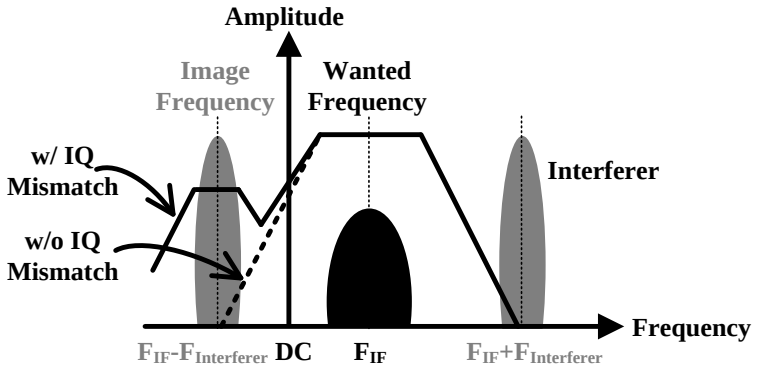

Figure 1. AC characteristics of low-IF receiver when IQ mismatch occurs.

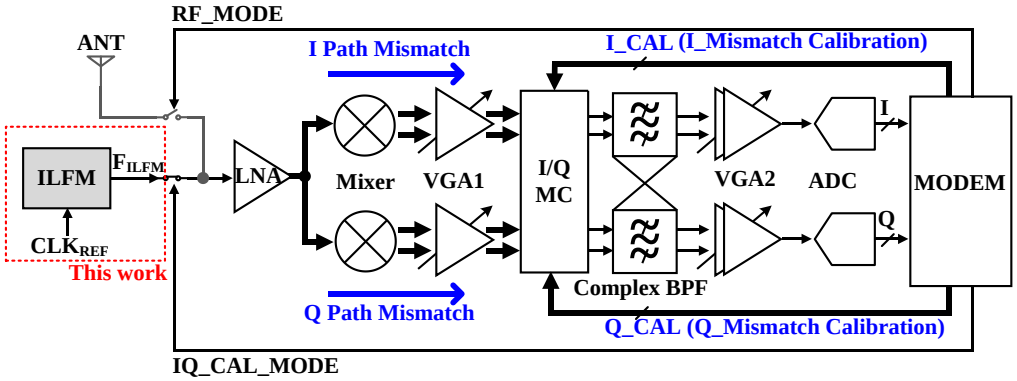

Figure 2. The block diagram of Low IF receiver with ILFM.

A subharmonic ILFM has been considered as a promising solution to generate a low phase noise and high-frequency clocks using limited silicon area and power consumption budget. It injects the reference clock into a Voltage Controlled Oscillator (VCO) and the injection signal realigns the output phase of the free-running VCO so that the low phase noise performance is acquired [7]. This phase-realignment mechanism with the reference clock allows the ILFM to have low jitter performance without a negative feedback system such as a Phase Locked Loop (PLL) or Delay Locked Loop (DLL). However, although the ILFM have many advantages, there is a critical requirement that the good phase noise performance can be achieved only when the target frequency of the ILFM is very close to the free-running frequency of the VCO. Therefore, the good phase noise performance of the ILFM might not be guaranteed, especially for ring oscillators whose free-running frequency is highly sensitive to Process, Voltage, and Temperature (PVT) variation. In addition, if the frequency of the Ring Oscillator is out of the lock range of ILFM due to the PVT variation, ILFM cannot achieve the injection locking [8]. Therefore, ILFM typically requires an effective PVT calibrator or calibration methods to mitigate the sensitivity of performance to the PVT variation.

The structure of the conventional and proposed ILFM, as shown Figure 3 [9]. Figure 3(a) shows a conventional ILFM structure with single-loop PLL. The PLL is used to calibrate PVT variation of VCO. However, the structure can't prevent the real-time frequency drift that is occurred by supply voltage and temperature variations. In addition, the structure has PLL loop path and injection path. It has timing problem because two paths are operated independently [10]. Figure 3(b) shows a dual-loop structure with a main oscillator and a replica oscillator [11]-[16]. The structure is proposed to resolve the timing problem of PLL based ILFM. The structure has two VCOs which are main VCO and replica VCO. The replica VCO is not injection lock to prevent the instantaneous frequency drift.

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The advantage of this method is that it can be calibrated with a frequency offset and PVT variation of the main VCO in real time using the replica VCO. However, if the mismatch is occurred between main VCO and replica VCO, the structure can't calibrate PVT variation. Also, the implementation is difficult because it consists of two loops, and there is a disadvantage in that the die area and power consumption are doubled compared to a single structure. Figure 3(c) shows the ILFM structure of an open loop type with Frequency Locked Loop (FLL). Figure 3(c) can reduce the power consumption by turning off the FLL block after F_{OUT} reaches the target frequency using FLL, and the area is small because only a simple FLL circuit is used.

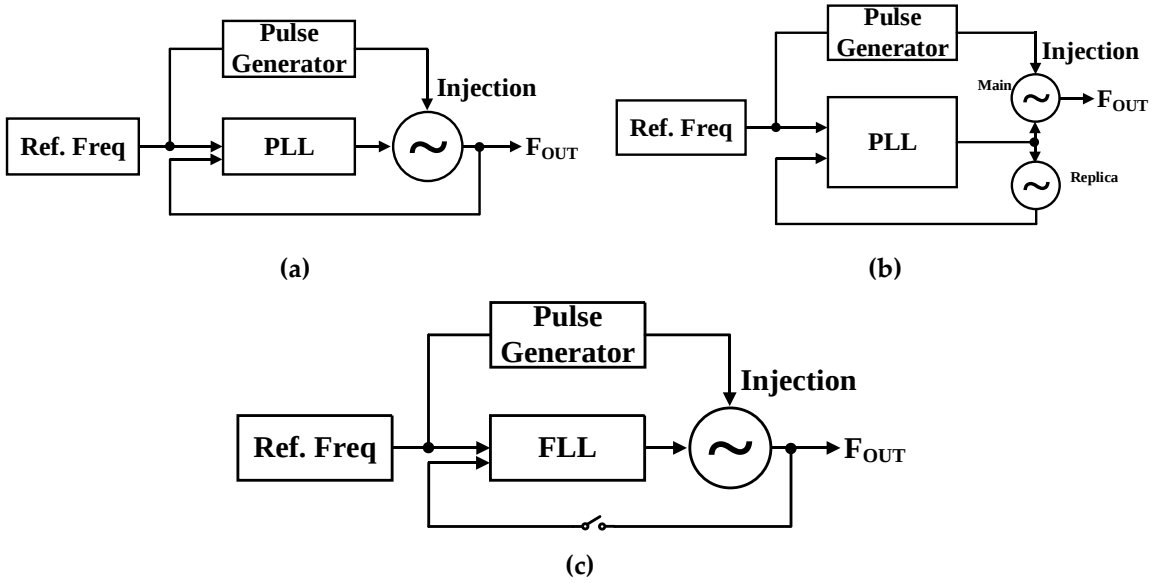

Figure 3. Structure of the ILFM **(a)** PLL based, **(b)** Dual-loop PLL based, **(c)** The proposed open-loop ILFM structure using FLL.

2. Injection Locked Frequency Multiplier (ILFM) With Frequency Tracking

Figure 4(a) shows a block diagram of the proposed ILFM. The proposed ILFM is composed of a Ring Oscillator, an Injection Generator, and FLL. Generally, the clock signal is required for calibration or other purposes in the transceiver or digital block. If the PLL is used to generate clock signal, and this places a burden on this system due to the additional area and power consumption. A Ring Oscillator is proposed instead of the PLL to satisfy the high frequency and low area.

The frequency of the Ring Oscillator is generated at close to the target frequency (f_{TARGET}). If the output frequency of the ILFM (f_{ILFM}) is near the f_{TARGET}, it is precisely locked to f_{TARGET} by the harmonics of the reference clock frequency (f_{ref}), 36 MHz [7].

$$f_{ILFM} = M \times f_{ref} \quad (1)$$

where f_{ILFM} is the output frequency of ILFM, and the multiplication factor M can be changed through the current control of the Delay Cell.

Figure 4(b) shows a schematic of the delay cell with an injection switch. The Delay Cell is composed of four inverters, a 6-bit Current Bank, and injection switches. A Ring Oscillator is proposed to acquire f_{TARGET}, as shown in Figure 4(a). The current bank is designed to adjust the frequency using Frequency Calibration Logic. Thus, it is possible to reduce PVT variations and, to reduce phase noise, the injection switches of M_{injt}, and M_{injb} are attached to the nodes of V_{on} and V_{op}, respectively.

Figure 5 shows the Frequency Calibration Logic of ILFM. It is composed of a 12-bit Counter, a finite-state machine (FSM), a Digital Comparator, a Coarse Tuning Controller, and a Fine Tuning Controller. Since the ILFM has a locked f_{TARGET} from the Injection Generator, the free running frequency must be close to the f_{TARGET}. Therefore, the role of the Coarse Tuning Controller is to set the frequency close to f_{TARGET}, by calibrating the free running frequency of the Ring Oscillator. The role of

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the fine tuning controller is to lock the ILFM in a f_{TARGET} by controlling the delay (ΔT) the of injection generator. When the frequency calibration logic is started, the 12-bit counter counts the current frequency of the Ring Oscillator. The counted value CNT_{ILFM}<11:0> is delivered to the digital comparator.

This result, CNT_{ILFM}<11:0>, is compared to the reference number, REF<11:0>, which is determined from Eqs. (2) – (3) based on the f_{TARGET}.

$$T\_EN_{CNT}(\mathrm{s}) = \frac{1}{f_{ref}(\mathrm{Hz})} \times 96 \tag{2}$$

$$REF<11:0> = \mathrm{T\_EN}_{CNT}(\mathrm{s}) \times f_{TARGET}(\mathrm{Hz}) \tag{3}$$

where T_EN_{CNT} is the value of the interval in which the EN_{CNT} signal is High. f_{ref} is the reference clock frequency (36 MHz), and f_{TARGET} is the target frequency.

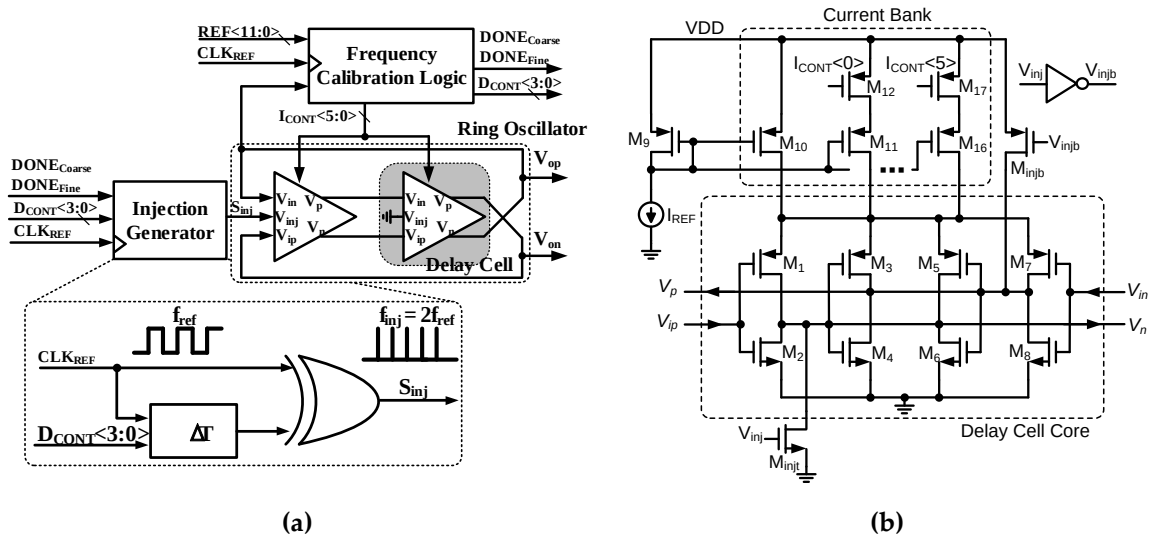

Figure 4. (a) Block diagram of proposed ILFM and **(b)** schematic of Delay Cell with injection switch.

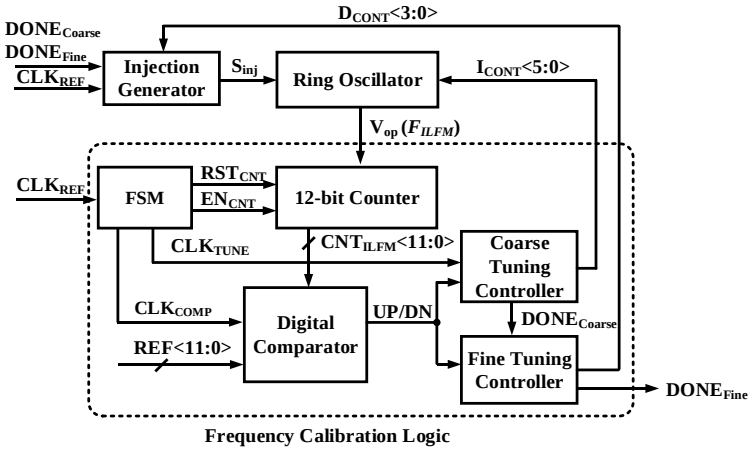

Figure 5. Block diagram of the Frequency Calibration Logic.

Figure 6(a) shows a flow chart of the Frequency Calibration Logic, and Figure 6(b) is a timing diagram of the FSM in the Frequency Calibration Logic. A 12-bit Counter is used to calculate the output frequency of the ILFM. It operates in an asynchronous way when a counter enable signal (EN_{CNT}) is high and is periodically reset by the counter reset signal (RST_{CNT}) generated by the FSM. The FSM determines the timing of the calibration by generating the decision clock (CLK_{TUNE}) and a comparison clock (CLK_{COMP}) using the CLK_{REF} signal [17].

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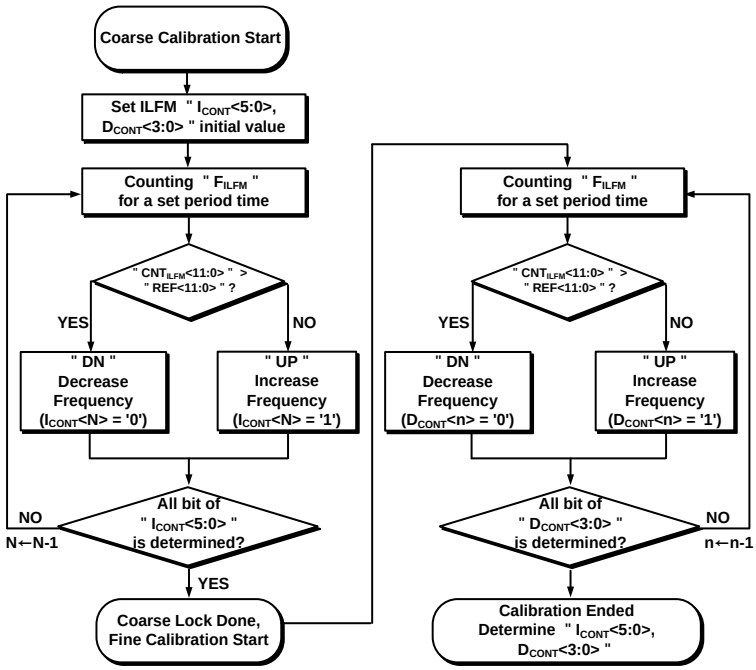
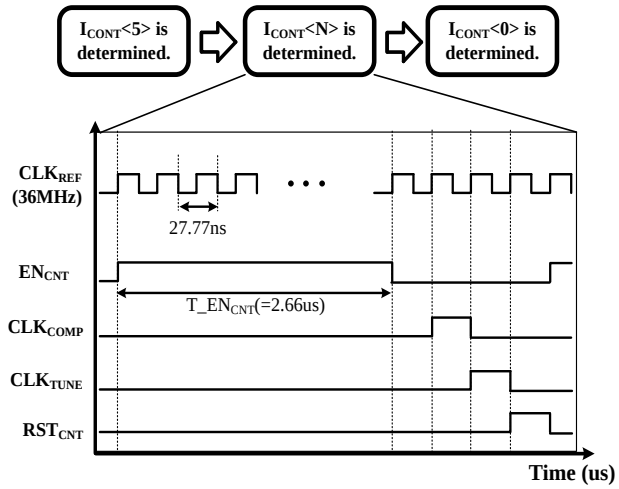


(a)



(b)

Figure 6. (a) Flow chart of Frequency Calibration Logic and **(b)** Timing diagram of 1-state of FSM in Frequency Calibration Logic.

If the value of CNTILFM<11:0> is higher than REF<11:0>, the DN is generated by the Coarse Tuning Controller and Fine Tuning Controller. On the other hand, if the value of CNTILFM<11:0> is lower than REF<11:0>, UP is generated. The calibration time is minimized by applying the binary search algorithm. Therefore, ICONT<5:0> is determined by the Coarse Tuning Controller after this loop has been operated 6 times. The fine tuning works in the same way as the coarse tuning, and the DCONT<3:0> values are determined when fine tuning is in progress. The DCONT<3:0> output determines the injection pulse width of the Injection Generator. The output frequency of the Ring Oscillator is sensitive to a PVT corner variation [7].

Figure 7(a) shows the simulation result of the frequency variation of the ILFM that is changed by the PVT variation. When Frequency Calibration Logic is not used, the output frequency of the ILFM changes from 766 MHz to 948 MHz depending on the corner condition.

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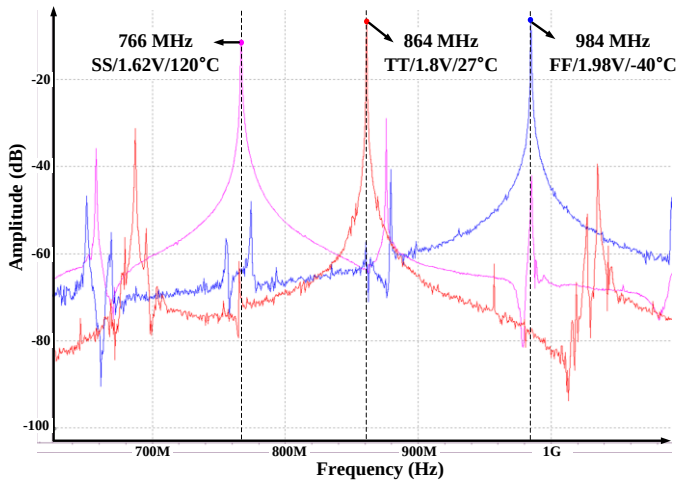
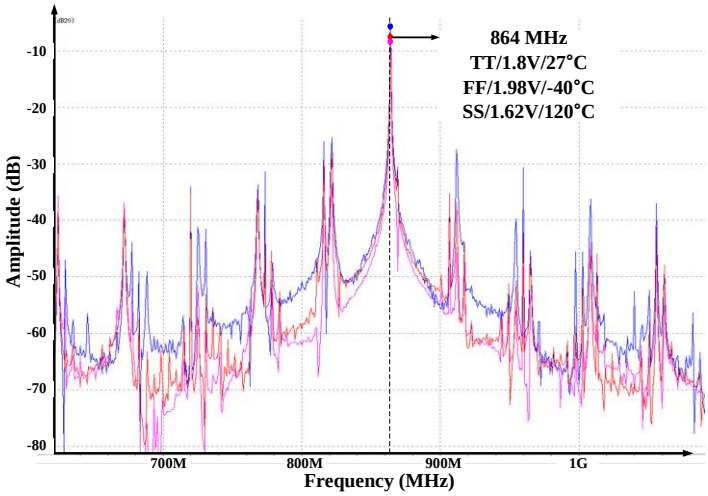
On the other hand, Figure 7(b) shows the simulation result when the proposed Frequency Calibration Logic is used, and the output frequency of ILFM is exactly calibrated to target frequency (846 MHz) at all PVT corner conditions.



(a)



(b)

Figure 7. The frequency of ILFM Frequency Calibration **(a)** before calibration and **(b)** after calibration.

3. Experimental Results

Figure 8 shows a chip microphotograph of the ILFM. The proposed design is fabricated in a 0.18 μm CMOS process and the area of the ILFM is 0.54 mm × 0.12 mm.

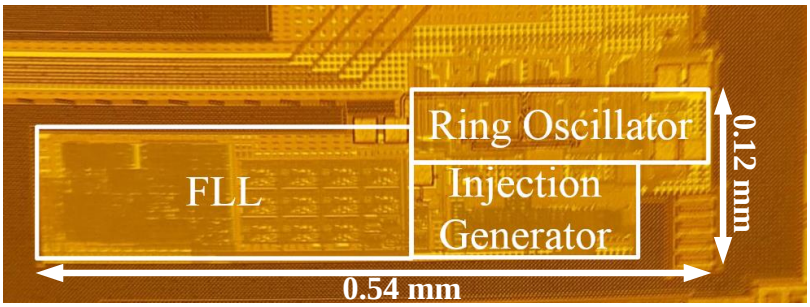


Figure 8. Chip microphotograph of ILFM

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Figure 9 is the ILFM top transient simulation result. As shown in the flow chart in Figure 8, find the target frequency while performing the FLL operation. After both the $DONE_{Coarse}$ and $DONE_{Fine}$ signals change to 'H', the CLK_{REF} signal is injected and injection locked to the target frequency.

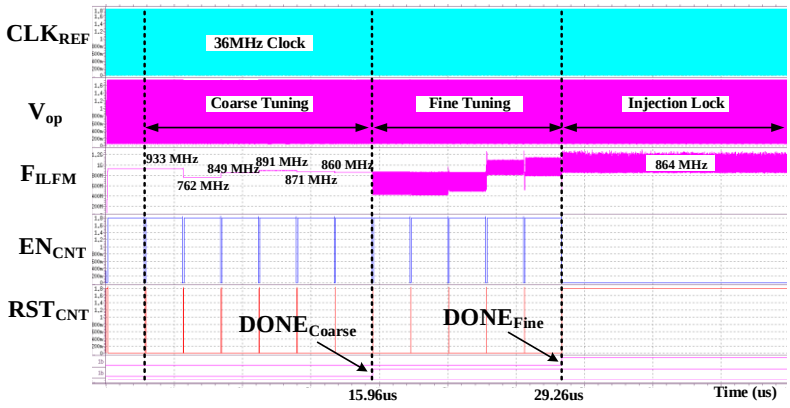

Figure 9. The top simulation of ILFM

Figure 10 shows the measurement results of the free-running frequency of the Ring Oscillator. The frequency of the Ring Oscillator can be adjusted in units of about 13 MHz and has a frequency range from 0.58 GHz to 1.41 GHz.

Figure 11 shows the measured injection locked full range of ILFM. The measured Injection lock range is form 612 MHz to 1152 MHz. After the Frequency Calibration operation, the ILFM can lock to N times the reference clock within the Injection Locked range.

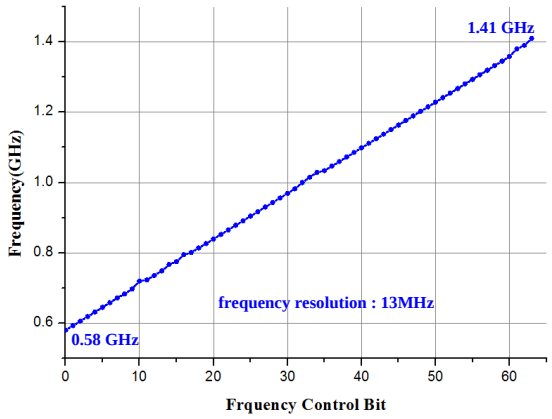

Figure 10. Free-running frequency range of Ring Oscillator.

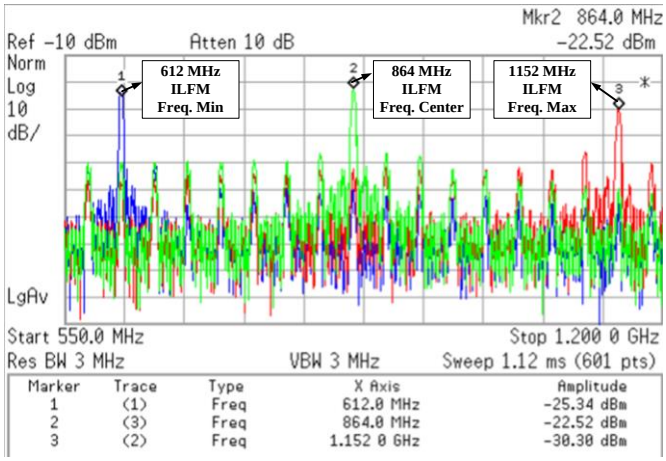

Figure 11. Injection Locked frequency range of ILFM.

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Figure 12 shows the measured phase noise of the injection locked in ILFM. When the short pulse is injected into the Ring Oscillator, the phase noise is -108 dBc/Hz at 1 MHz offset. When the ILFM is locked by injection, the phase noise is reduced more than the free-running noise. With the effect of the injection, in-band phase noise is also reduced.

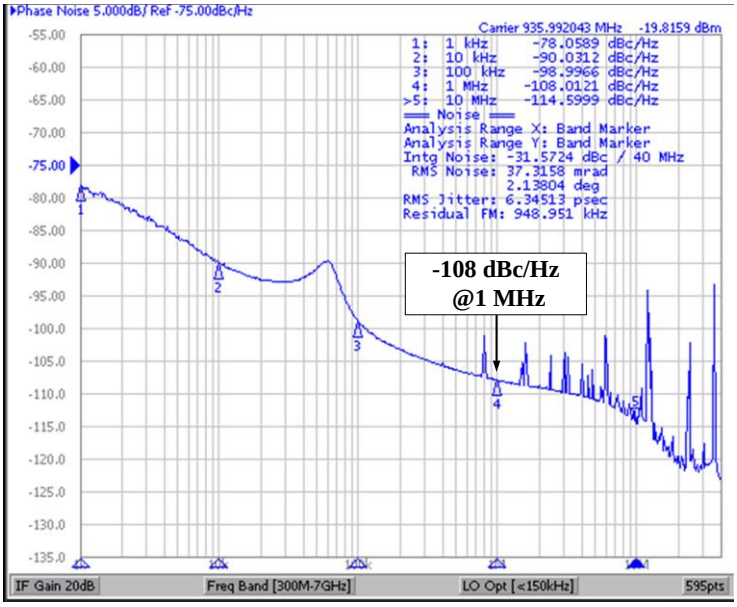

Figure 12. Measurement of injection locked phase noise at center frequency.

Table I shows the comparison with published papers ([18]-[20]). The proposed paper is designed to make an RF signal to the RF frontend before the RF signal is input from the antenna. RF signals for calibrating I / Q mismatch do not require ultra-low jitter performance. The reference spur is generated by the ILFM, and it is attenuated by the BaseBand Filter. The performance of the proposed paper with the highest priority is the silicon area and current consumption. The definition of FOM is defined as follows:

$$FoM = 10 \cdot \log\left(\left(\frac{Jitter_{RMS}}{1s}\right)^2 \cdot \left(\frac{P_{diss}}{1mW}\right)\right) \quad (4)$$

where $Jitter_{rms}$, 1s, and P_{diss} are the RMS jitter value of ILFM output, 1 second, the power consumption, respectively [20].

Table 1. Performance Comparison of ILFM

	[18]	[19]	[20]	**This work**
Process (nm)	180 nm	65 nm	65 nm	**180 nm**
Topology	IL+ Open Loop	IL+ DPLL	IL+ DPLL	**IL+ FLL**
Output Frequency (GHz)	1.88	0.576-0.608	2.5-5.75	**0.612–1.152**
Reference Frequency (MHz)	80	32	125	**36**
Phase noise (dBc/Hz @1MHz offset)	-122	-114	-115.9	**-108**
$Jitter_{rms}$ (ps) (Integ. Range)	N/A	4.23 (100 Hz ~ 40MHz)	0.34 (10 kHz ~ 40MHz)	**6.3 (1kHz ~40MHz)**
Power consumption (mW)	55	10.5	5.3	**0.95**
Active area (mm^2)	0.31	0.158	0.158	**0.0648**
FoM (dB)	N/A	-217	-242.4	**-194.2**

4. Conclusions

This paper presents a 612-1152 MHz Injection Locked Frequency Multiplier (ILFM). The proposed ILFM is only used for sending an input signal to the receiver in the I/Q mismatch calibration mode. Using the Phase-Locked Loop (PLL) to calibrate the receiver places a burden on this system due to the extra area required and power consumption. Instead of the PLL, to satisfy high frequency, low jitter, and low area, a Ring Oscillator is proposed. The free-running frequency of the ILFM is automatically digitally calibrated to reflect the frequency of the injected signal from the harmonics of the reference clock. To control the frequency of the ILFM, the load current is digitally tuned with 6-bit digital control signal. The proposed ILFM locks to the target frequency using a digitally controlled Frequency Locked Loop (FLL). This chip is fabricated using 1-poly 6-metal 0.18 μm CMOS and achieve the wide tuning range of 612~1152 MHz. The power consumption is 0.95 mW from a supply voltage of 1.8 V. The measured phase noise of the ILFM is -108 dBc/Hz at a 1 MHz offset.

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Author Contributions: Kang-Yoon Lee guided and directed the authors for this work. SungJin Kim and Dong-Gyu Kim studied, proposed and designed the overall architecture of Open Loop ILFM with FLL. They wrote the paper. Chanho Kim, Dongsoo Lee and Sang-Sun Yoo contributed in making the layout of the proposed architecture. Keum Cheol Hwang guided the antenna and measurments. Young Gun Pu performed the measurements with SungJin Kim, Dong-Gyu Kim and Chanho Kim. Youngoo Yang and Minjae Lee designed the related top architecture.

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