Article

New Switched-Dual-Source Multilevel Inverter for Symmetrical and Asymmetrical Operation

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Abstract: The past two decades has seen a growing demand for high-power, high-voltage utility scale inverters mostly fueled by the integration of large solar PV and wind farms. Multilevel inverters have emerged as the industry choice for these megawatt range inverters because their reduced voltage stress, capable of generating an almost sinusoidal voltage, in-built redundancy, among others. This paper present a new Switched-Source Multilevel Inverter (SS MLI) architecture. The new inverter show superior over existing topologies. It has reduced voltage stress on the semiconductor, uses less number of switches –reduced size/weight/cost and increased efficiency. The new SSMLI is comprised of two voltage sources (V_1, V_2) and 6 switches. It is capable of generating 5-level output voltage in symmetric modes (i.e., $V_1 = V_2$), and 7-level output voltage in asymmetric modes (i.e., $V_1 \neq V_2$). To demonstrate the validity of the proposed inverter, simulations results using MATLAB®/Simulink® for 5- and 7-level output voltages are presented . The simulations are also verified experimentally using a laboratory prototype.

Keywords: multilevel; inverter; single phase; reduced switch-count; h-bridge.

1. Introduction

The past couple of decades has seen huge investments in renewable resources (RES) as a way to reduce carbon footprint. These initiatives have resulted, in recent years, in the installation of utility scale wind and solar PV farms. The operations of such MW-scale plants require high voltage/power multilevel inverters (MLIs), leading to the proliferation of MLI [1,2]. MLIs can be categorized into three types:neutral-point-clamped (NPC) [2,3], flying-capacitor (FC) [4,5], and cascaded H-bridge (CHB) topologies[6,7]. Some research have also proposed hybrids of the above types [8,9]. The main advantages of MLIs over their traditional 2-level counterparts are improved power quality, reduced filter requirements, lower electromagnetic interference, and lower dv/dt stress on loads [10,11].

A shortcoming of NPC topology is an unbalance of the neutral point leading to uneven thermal distribution among the semiconductor devices, increase in harmonics, and reduction of power quality [12]. FC inverters also suffer from capacitor voltage imbalance issues, which lead to a deterioration of power quality and an increase in blocking voltages. They also require larger capacitor banks and additional pre-charging circuitry. CHB MLIs suffer from input DC leakage current that could damage, for example, PV panels and pose safety problems [13,14]. However, CHB topology has a lot of advantages – modularity, fewer number of components,symmetric and asymmetric operating modes (i.e., equal and unequal DC sources), etc.

Many recent studies on the CHB topology have focused on generating more voltage levels by using switched-capacitor (SC) or switched-source (SS) MLI configurations. The SC MLIs [15,16] aim to produce more output voltage levels with a single or minimal number of power supplies and a series of self-balancing capacitors. However, they suffer from increased voltage stress on the switches and power dissipation in the increasing number of series diodes [15]. Several SS MLIs are proposed in [7,17]. Unlike the SC configuration where capacitors are switched in series/parallel combinations, the

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SS configuration uses instead multiple DC sources to achieve the voltage levels. This configuration is inherently suited for applications where there are multiple DC sources such as in battery storage, solar PV or fuel cells. In the SS configuration, a higher number of voltage levels can be obtained when the DC sources have different amplitudes (asymmetric operation) [18] than the symmetric topology (all DC sources have the same amplitude) using the same number of components (sources, switches, and passive devices). Additionally, the current commutation path is generally shorter in the SS topology than in the SC topology; thereby, reducing power dissipation. Another advantage of SS MLIs over SC MLIs is the high number of redundant switching states which may be useful for certain control applications,e.g., fault-tolerant inverters.

In this paper, a new SS MLI topology is proposed. The new topology exhibits better performance, when compared to similar SS MLI topologies, in terms of the number of switches, current commutation path, and voltage stress on the switches. The validity of the proposed topology is verified by MATLAB®/Simulink® simulations. The rest of the paper is organized as follows: The structure and operation of the inverter is presented in Section 2. Comparisons among the topologies is discussed in Section 3, and simulation results are presented in Section 4. Finally, conclusions are drawn in Section 5.

2. Architecture and Principle of Operation

2.1. Architecture

The basic unit of the proposed MLI (see Fig. 1) is comprise two DC power sources (V_1 and V_2), four unidirectional switches (S_1, S_2, S_3 and S_4), and two bidirectional switches (S_5 and S_6). This basic unit, it is capable of generating 5-level output voltage (i.e., V_{ab}), when $V_1 = V_2$ (i.e., symmetric mode operation), and 7-level output voltage when $V_1 \neq V_2$ (i.e., asymmetric mode operation). The basic unit can be cascaded to generate more voltage levels. If m number of basic units are cascaded as shown in Fig. 2 , the inverter can generate up to $(2^{m+1}+1)$ and $(2^{2m+1}-1)$ $(m = 1,2,3,\ldots)$ output voltage levels for symmetric and asymmetric operations, respectively.

In order to avoid short-circuiting of the DC power sources, only one of the left side switches (i.e., S_1, S_3, S_5) can conduct at any instant. Similarly, only one of the right side switches (i.e.,S_2, S_4, S_6) can be ON at the same time. That is,

$$S_1 + S_3 + S_5 = 1;\ S_2 + S_4 + S_6 = 1 \tag{1}$$

where S_k denotes the switching function of switch k ($k = 1,2\ldots,6$), and takes the value of 1 when ON, and 0 when OFF. Based on (1), Table 1 shows all the switching states of the basic unit and the resulting inverter output voltage. It consists of three null states Based on (1), Table 1 shows all the switching states of the basic unit and the resulting inverter output voltage. It consists of three null states (i.e.,

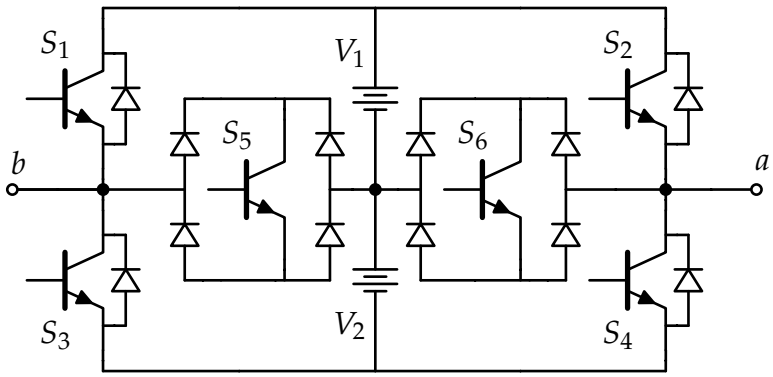

Figure 1. Structure of the proposed topology as standalone.

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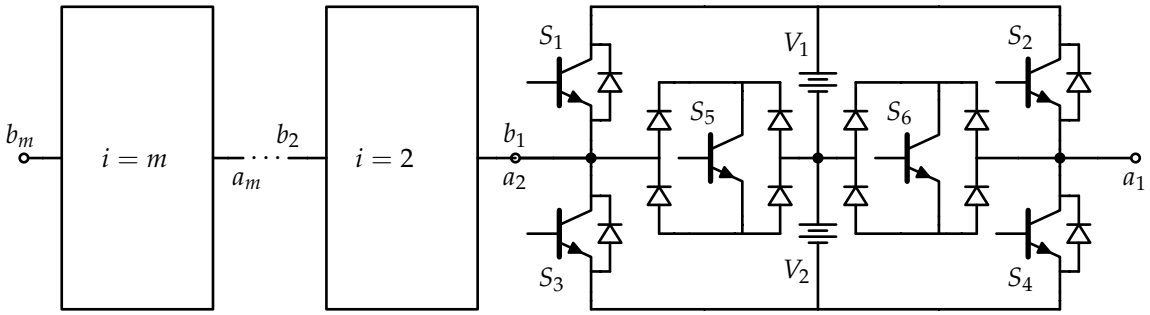

Figure 2. m cascaded units to generate more voltage levels.

Table 1. Switches states for basic unit

States	S_1	S_2	S_3	S_4	S_5	S_6	V_{ab}
1	0	0	1	1	0	0	0
2	0	0	1	0	0	1	$+V_2$
3	0	0	0	1	1	0	$-V_2$
4	0	0	0	0	1	1	0
5	0	1	1	0	0	0	$+(V_1+V_2)$
6	0	1	0	0	1	0	$+V_1$
7	1	0	0	1	0	0	$-(V_1+V_2)$
8	1	0	0	0	0	1	$-V_1$
9	1	1	0	0	0	0	0

$V_{ab} = 0V$) and six active states. The three redundant null states may b utilized to achieve different control objectives. The authors did not investigate this in this paper. In Table 1, the states shown in light-gray (i.e, all except 4) are the states utilized in this paper. The bidirectional switches protect the inverter from short circuits when it operates in asymmetrical mode.

The use of bidirectional switches distorts the output waveform (at low voltage levels, but is insignificant at medium high voltage level applications) due to the voltage drop in each one of the diodes of the rectifier bridge (two diodes forward biased simultaneously, $V_{drop} \approx 2 \times 0.7 = 1.4\ V$). and six active states Table 1 shows that there are three redundant null states ($0V$ output). The states shown in light-gray are the ones used in this paper. The bidirectional switches protect the inverter from short circuits when it operates in asymmetrical mode. The use of bidirectional switches distorts the output waveform (at low voltage levels, but is insignificant at medium high voltage level applications) due to the voltage drop in each one of the diodes of the rectifier bridge (two diodes forward biased simultaneously, $V_{drop} \approx 2 \times 0.7 = 1.4\ V$).

2.2. Operation principle

The generation of the multilevel voltage output is based on the switching states given in Table 1. For example, to produce a 7-level output (V_{ab}), at least one null state (i.e., state **1**, **4** or **9**) and all the active states (i.e.; **2**, **3**, **5**, **6**, **7**, and **8**) are fired in a sequence to achieve the 7-level output. For uniform power dissipation among the six switches, two null states (i.e., **1** and **9**) are utilized; with state **1** during the positive half-cycle and state **9** in the negative half-cycle. The Phase Disposition PWM (PD-PWM) is selected based on its superior performance [19], but any PWM method may be used to control the semiconductor switches. Fig. 3 show the current commutation for each switching state. For example, to produce $(V_1 + V_2)$ in the positive half-cycle, switches S_1 and S_3 must be turned ON (i.e., state **5** in Table 1). The current flow is as shown in Fig. 3e. Fig. 3 show the current commutations for all the 7 voltage levels. Note that if $V_1 = V_2$, a maximum of 5-level output can be realized.

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3. Comparison with similar topologies

In this section, the proposed topology is compared with the topologies presented in [20,21], and the conventional cascaded H-bridge topology also discussed in [21]. The comparison is made in terms of (i) total number of semiconductor devices , (ii) number of active components in current path (conduction losses) and voltage stress that each switch will be required to handle.

3.1. Number of semiconductor devices

The number of semiconductor devices have an impact on the cost and size/weight of the MLI unit; being able to generate the same number of voltage levels in the output of the inverter by using less number of switches will lower cost and at the same give a compact inverter. Fig. 4a and Fig. 4b show the number of switches (N_{sw}) needed to generate the same number of voltage levels (N_l) in the output for the different topologies in symmetric and asymmetric mode respectively. In symmetric mode (Fig. 4a), it is obvious that the proposed proposed topology outperforms the 3 other topologies with the lowest switch count for the same voltage level. In asymmetric mode (i.e., Fig. **??**, however, the proposed topology fares better at lower voltage levels ($N_l \leq 50$), but this advantage diminishes at higher voltage levels.

3.2. Number of semiconductors in current path

Unlike in deal cases when we assume a switch or diode can turn-on or turn-off instantaneously without any power loss, real semiconductor switches have a finite switching transition time. This finite transition period is accompanied by power losses transients [22]. Hence, the less number of switches required to produce a voltage level implies less power losses. Fig. 5a and Fig. 5b show the number of switches in the current path for the same voltage levels for the different topologies in symmetric and asymmetric mode respectively. The proposed topology performs better than in both modes resulting in higher efficiency at every voltage level.

3.3. Total standing voltage

Another important factor that should be taken into consideration when comparing the topologies is the minimum voltage rating of the switches. This minimum voltage rating, which will influence on the price and size of the switches, is related to the voltage stress that they need to handle in blocking state. This is also called standing voltage and the total standing voltage is obtained by addition of the blocking voltage requirement of each switch of a topology.

For comparison purposes, a value of $1V$ was assumed for V_{dc}. Fig. 6a and Fig. 6b show the total standing voltage in symmetric and asymmetric modes respectively for all the topologies. In both symmetric and asymmetric modes, it can be shown that the proposed topology outperforms all others topologies.

4. Simulation and Experimental Results

Fig 7 shows a laboratory prototype built to validate the proposed topology. Simulations were carried out using MATLAB/Simulink. The semiconductor switches are IGBT IXGN120N60A3D1 with voltage and current ratings of 600 V, 120 A, respectively. The gate control signals were implemented using OPAL-RT OP5700 RCP/HIL FPGA-based Real-time Simulator. Two low power DC sources were engaged in supplying the required voltages. Table 2 list specifications of the inverter used for both simulations and experiment.

Fig. 8a shows the simulation results of the converter output voltage and load current waveforms the 5-level (symmetrical) operation. The THD of the voltage and current waveforms are 28.08% and 1.46%, respectively. The corresponding experimental waveforms for the symmetrical operations are shown in Fig. 8b. The experimental waveforms confirm accurate 5-level output voltage, having a current waveform with small THD. The results of the asymmetrical operation (7-level) are presented in

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Table 2. Parameters for 7-level and 31-level simulations.

Parameter	Value
Frequency f	60 Hz
Switching Frequency f_s	2340 Hz
Modulation Index m_a	0.95
DC power sources (5-level)	$V_1 = 30\ V\ V_2 = 30V$
DC power sources (7-level)	$V_1 = 40\ V\ V_2 = 20\ V$
Load	$R = 250\ \Omega; L = 350\ mH$

Fig. 9. Fig. 9a) show simulated voltage and current waveforms whilst Fig. 9b present the corresponding experimental waveforms. The THD of the voltage and current waveforms for the 7-level operation are 19.00% and 1.13%, respectively. As in the case of the symmetrical operation, the experimental waveforms confirm accurate 7-level output voltage, with an almost sinusoidal current waveform. The presented results clearly verify the feasibility of the proposed inverter topology.

5. Conclusions

In this paper, a new topology for switched-source multilevel inverter (SS MLI) has been proposed. The structure and principle of operation are discussed and validated by both theoretical simulations and experiments. The basic unit can operated in symmetric and asymmetric modes. The new SS MLI topology is compared to three similar SS MLI topologies in terms of the number of switches required to generate a voltage level, the number of switches in current path (power losses) and total standing voltage the switches need to handle. The proposed topology outperforms the other topologies in most of the scenarios, presenting a significant reduction on the total cost and size of the unit, as well as a reduction in power losses. MATLAB/Simulink simulations and experiments using a laboratory prototype are presented for 5- and 7-level operations.

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Author Contributions: Cristopher Luciano and Kennedy Aganah conceived and designed the experiments; Cristopher Luciano performed the experiments; Cristopher Luciano, Kennedy Aganah and Mandoye Ndoye wrote the paper; Gregory Murphy contributed supplies/simulation tools;

Conflicts of Interest: The authors declare no conflict of interest.

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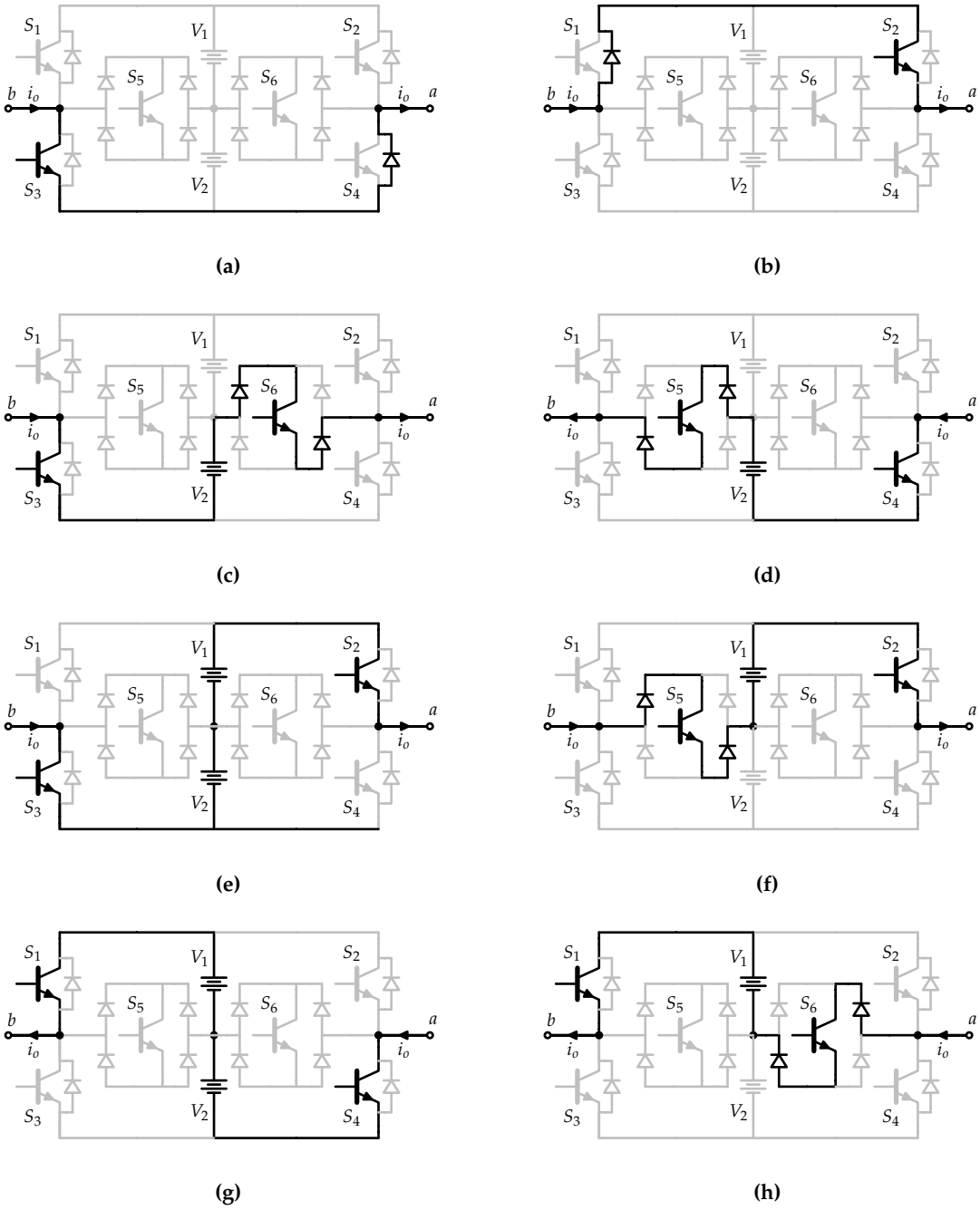

Figure 3. Structure of the proposed topology as standalone.

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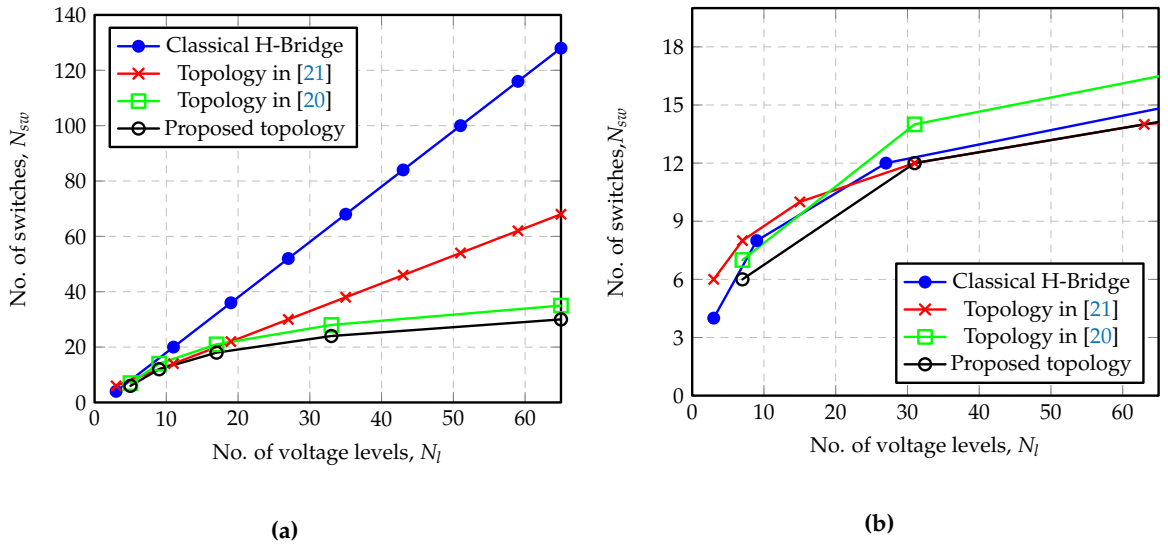

Figure 4. Number of switches vs. output voltage levels of proposed inverter compared with 3 other topologies in (a) symmetric mode and (b) asymmetric mode.

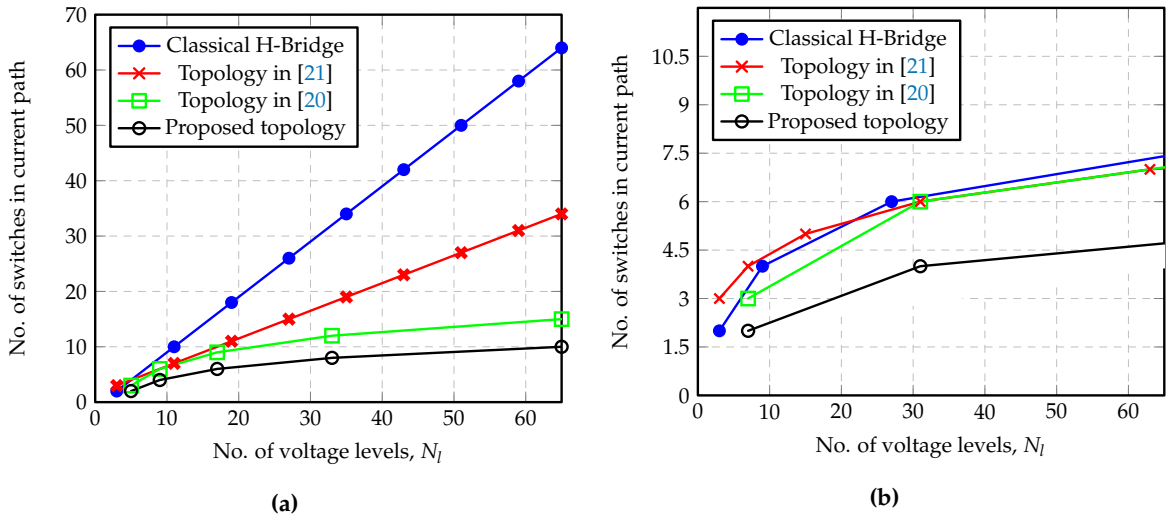

Figure 5. Number of switches in current path vs. output voltage level of proposed inverter compared with 3 other topologies in (a) symmetric mode and (b) asymmetric mode.

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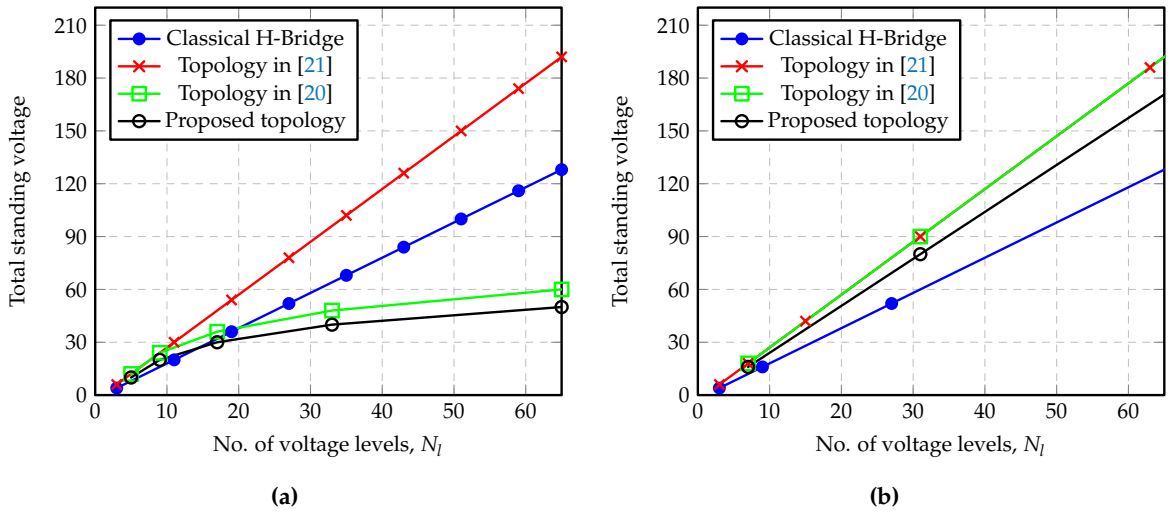

Figure 6. Total standing voltage vs. output voltage levels of proposed inverter compared with 3 other topologies in (a) symmetric mode and (b) asymmetric mode.

Figure 7. Picture of experimental test set-up

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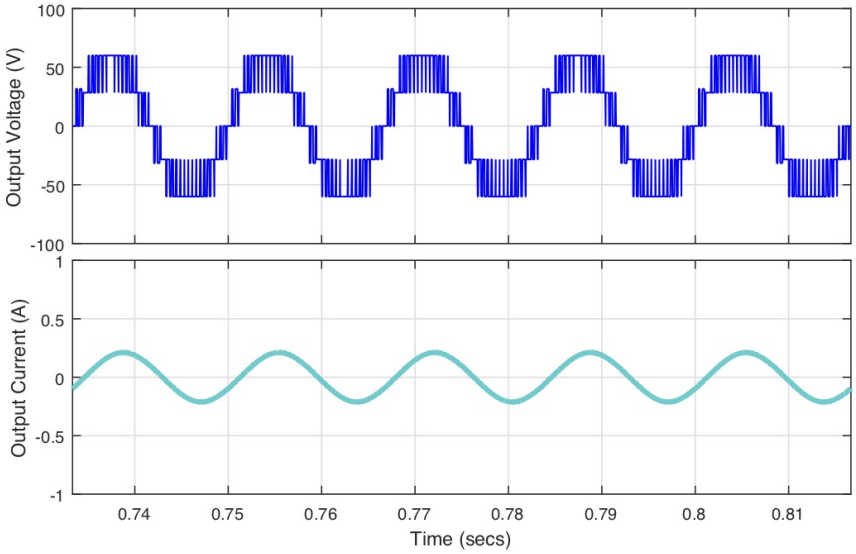
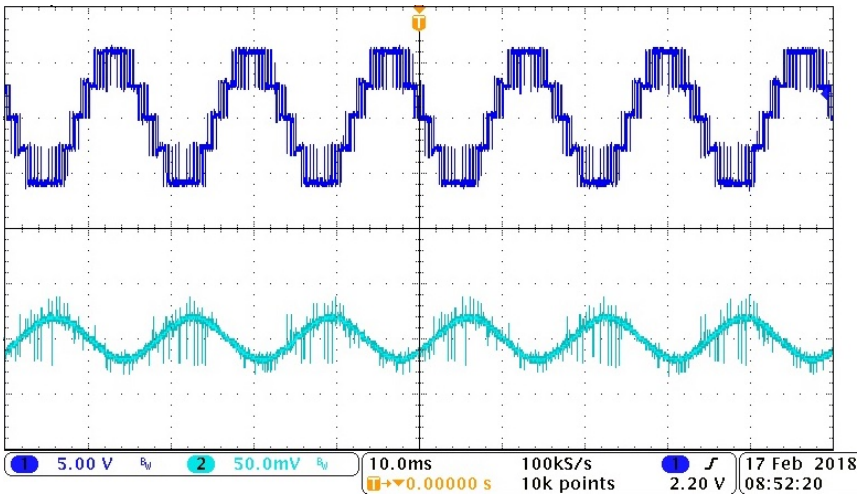


(a)



(b)

Figure 8. Results of 5-level SSMLI: (a) Simulated output voltage (top) and load current (b) experimental output voltage (top, 25V/div) and current (bottom, 0.25 A/div).

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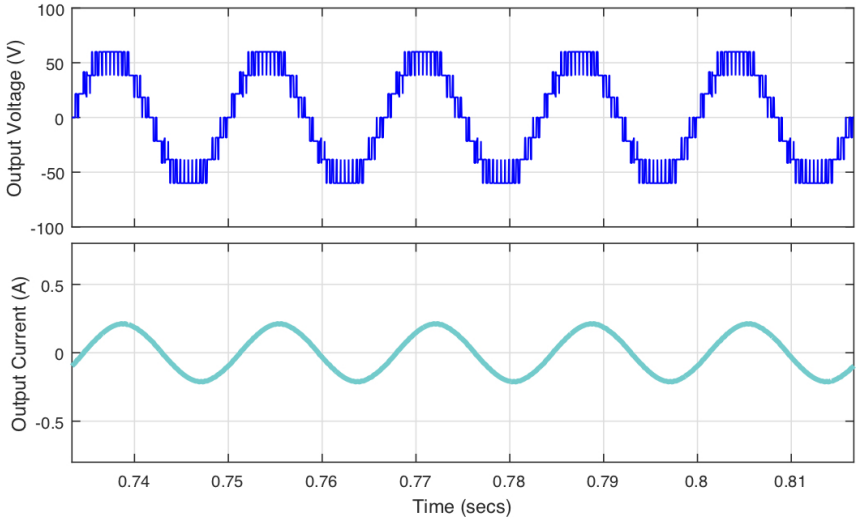

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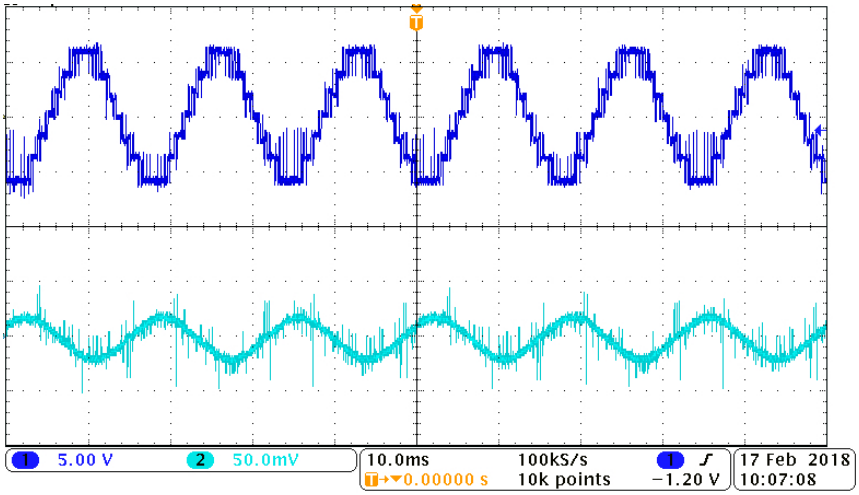

(b)

Figure 9. Results of 7-level SSMLI: (a) Simulated output voltage (top) and load current (b) experimental output voltage (top, 25V/div) and load current (bottom, 0.25A/div).