Article

None Operational Amplifier (OPA) Based: Design of Analogous Bandgap Reference Voltage

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Abstract: By using 0.35-um CMOS process, this work achieves a design of analogous band-gap reference voltage circuit with low temperature coefficient. The proposed circuit operates at 3V and generates a reference current of 44 uA. The HSPICE simulation results show the temperature coefficient of this circuit is 23 ppm/　at range of -10　 to 100　, and the line regulation (the ratio of output current variation to supply voltage variation) is estimated as 1.95 uA/V from supply voltage variation of 3 V to 5 V. The experimental chip is fabricated and measured. The circuit provides adjustable capability for output voltage among temperature variation of -10 - 100　. The chip area is 　534 × 695 　um². In this new design, the operational amplifier is not necessary. The chip design effort can be great reduced.

Keywords: Band-gap voltage reference; voltage reference; circuit design

1. Introduction

Because of the convenience and portability, more portable consumer electronic devices are frequently used today. There are always tens to hundreds of chips co-operation within these consumer electronic devices. In order to further shrink device size and toward lightweight continuously, more electronic elements are expected to be integrated into a chip to realize the system almost functions. As a result, the function of chip trends towards from single specific to system multiple functions. In general, a system-embedded-on-a-chip (SoC) has multiple voltage sources or voltage references within chip design. The capability of voltage reference is with low output voltage/current variation in spite of variety of temperature, supply voltage, and noise interfered. Therefore, the voltage reference circuit currently has been widely used in analog circuit, digital circuit and mixed-signal circuit, such as operational amplifiers, analog-to-digital converters (ADC), digital-to-analog converters (DAC), phase locked loop (PLL) circuits and power regulators. In open literature, many circuit schemes for voltage reference and its improved versions have been proposed [1-8] in recent years. The performance of voltage reference will dominate the system function. The design of internal voltage reference circuit becomes more important especially for in SoC era. Currently, the most popular circuit scheme is bandgap voltage reference.

The basic circuit for bandgap voltage reference is shown in Fig. 1. The bootstrapping circuit makes the potential voltage of nodes 'a' and node 'b' as equal as possible, to reduce the effects of channel length modulation and supply voltage variation. It uses emitter-base voltage difference between two bipolar junction transistors (BJTs) to generate a positive temperature coefficient (PTC) current. In conventional CMOS technologies, these BJTs are parasitic transistors. After that, it uses current mirror architecture (M3/M4/M5) to copy the PTC current to the output resistor R_L. The voltage

drop V_{RL} is added to V_{EB} of BJT with negative temperature coefficient to generate a stable reference voltage output.   Finally, the objective of the basic circuit is to form a precise and stable voltage reference in spite of temperature variations and supply voltage fluctuations. The output of bandgap reference circuit shown in Fig. 1 is given as

$$V_{ref} = V_{EB} + \Delta V_{EB} \left(\frac{R_L}{R_1} \right). \tag{1}$$

V_{EB} is with negative temperature coefficient, and ΔV_{EB} related to thermal voltage V_t (that is, kT/q) is with positive temperature coefficient. The temperature effects of V_{EB} and ΔV_{EB} are about -2.5 mV and +0.085 mV per centigrade degree respectively. According to the proper ratio settings of R_L, R_1, and the area matching in BJTs, temperature effect of output voltage can be canceled drift out each other. Therefore, output V_{ref} in theoretically can be obtained in independent of temperature.

However, the voltage on nodes 'a' and 'b' in Fig. 1 is not identical potential due to the channel length modulation and body effects. The temperature coefficient of basic scheme is a little bit large. Another conventional bandgap reference voltage circuit is shown in Fig.2. An operational amplifier is embedded in the circuit to provide nearly equal voltage between two input nodes. The output voltage of bandgap reference circuit is also given as Eq. 1. In despite of Figs. 1 and 2, the ratio of R_L and R_1 is always to set a proper value to keep the output voltage temperature insensitivity.
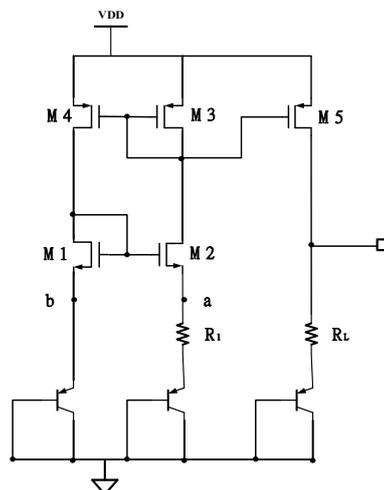

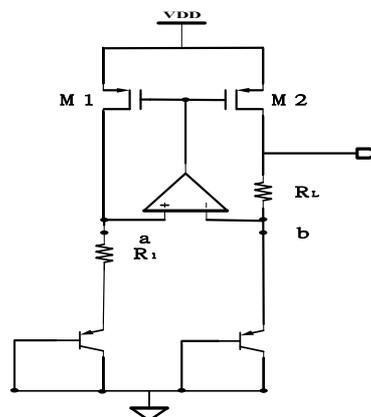**Figure 1.** Basic bandgap reference voltage circuit.

Figure 2. Another basic bandgap reference voltage circuit (with opa)

Based on Fig. 2 scheme, an improved circuit for output voltage adjustable is achieved as Fig. 3 [1]. The circuit makes the output reference voltage can be altered by using various resistors ratios. In contrasting to Fig. 2, an additional operational amplifier and current mirror are extra used in Fig. 3. Due to high-gain operational amplifier, voltage on nodes 'b' and 'c' are equal. The current of M3 is

V_{EB}/R_2 with negative temperature coefficient. By M3/M4 current mirror, the current of M4 is $(V_{EB}/R_2)(W/L)_{M4}/(W/L)_{M3}$. After M4/M5 current summation, the voltage of the output resistor R_L can be derived as

$$V_{ref} = R_L \left(\frac{V_{EB}}{R_2} \frac{(W/L)_{M4}}{(W/L)_{M3}} + \frac{\Delta V_{EB}}{R_1} \frac{(W/L)_{M5}}{(W/L)_{M2}} \right). \tag{2}$$

The desired output voltage Vref can be obtained by settings of various resistances and aspect ratio of transistors. However, two operational amplifiers are needed in this design. In general, the design of operational amplifier with high performance in chip realization is difficult by using conventional process.
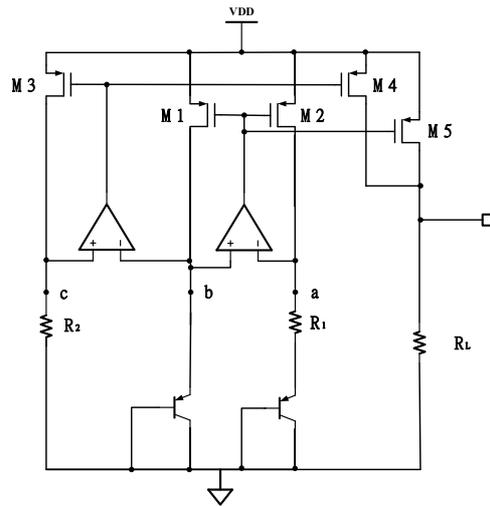
Figure 3. The bandgap reference voltage with adjustable capability [1].

2. Circuit Design

In consideration of the following two issues: first, the output voltage of conventional band-gap reference circuit is always limited to around 1.25 V, due to the constant ratio of negative temperature coefficient of V_{EB} and positive temperature coefficient of ΔV_{EB}. The second issue, a high performance operational amplifier is not easily realized in chip. In addition, the overall circuit complexity and power consumption are resulted in increased due to these more electronic elements. In this study, bandgap reference voltage circuit without needing operational amplifier is redesigned and inspected. The new schematic diagram of the circuit is shown in Fig. 4.

The current mirror function is achieved by M1/M4/M6/M7 to make nodes 'b' and 'c' voltage as equipotential as possible. Due to the equipotential, the current flows through resistor R_2, $I_{R2}=V_{EB}/R_2$, which is a negative temperature coefficient current. The current mirror of M6 and M8 is used to copy the current and addition of the positive temperature coefficient current I_{M5}. Finally, the output current with nearly zero temperature coefficient will be expected to arrive. The expression of the bandgap reference voltage is given as

$$V_{ref} = R_L \left(\frac{V_{EB}}{R_2} \frac{(W/L)_{M8}}{(W/L)_{M6}} + \frac{\Delta V_{EB}}{R_1} \frac{(W/L)_{M5}}{(W/L)_{M3}} \right). \tag{3}$$
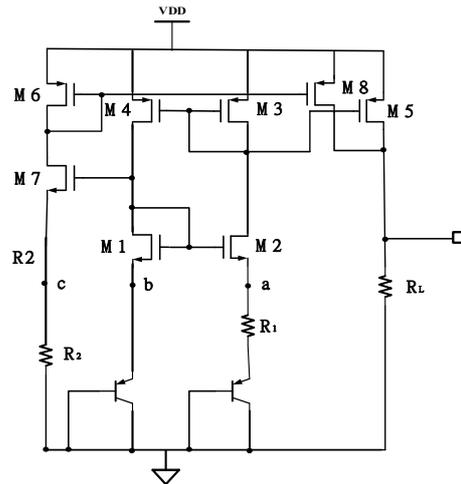
Figure 4.   The proposed bandgap reference voltage circuit without needing of operational amplifier.

A start-up circuit is needed to avoid a zero output current (another stable bias point) held in circuit initial phase. The whole circuit including start-up circuit is shown in Fig. 5. Transistors M9-M11 try to achieve a none zero current I_D in transistors M1 and M2 when the circuit is initially powered up.
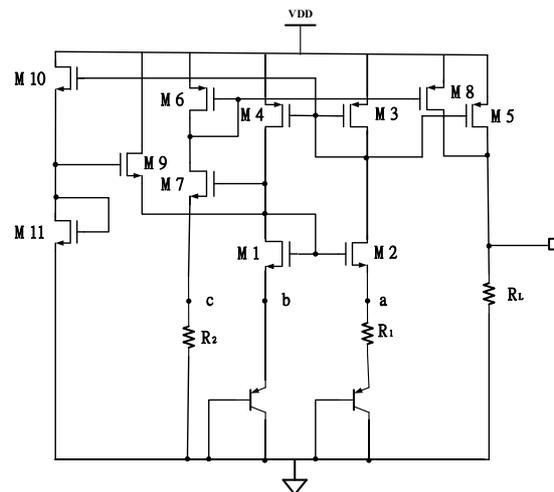
**Figure 5.** The whole proposed bandgap reference voltage circuit.

3. Simulation and Chip Measured Results

Based on TSMC 0.35-μm CMOS process, the whole circuit shown in Fig. 5 is simulated by using HSPICE simulation program. HSPICE is a very popular circuit simulator in chip design, and nearly it is a de facto standard to verify circuit function. Figures 6 to 13 show the simulation results. Figure 6 shows the line regulation of output current when supply voltage varies from 3 V to 5 V. In Fig. 6, the output current of the circuit is 44.8 μA at 3-V supply voltage and 48.7 μA at 5 V. The line regulation for output current is estimated as 1.95 μA/V.

Another important factor for bandgap reference: temperature coefficient will be inspected. When the loading is altered and varied, the circuit is still function works within reasonable low temperature coefficients. We use various loading resistances of 1 Ω, 10 Ω, 100 Ω,1 kΩ, 10 kΩ, 20 kΩ and 30 kΩ to inspect the output voltage variation when temperature is varied from −10   to 100 . Under R_L loading of 1-Ω, Fig. 7 shows the output voltage variation in temperature of −10   to 100 . The maximum output reference voltage is 44.841 μV and the minimum output reference voltage is 44.728 μV. The temperature coefficient (TC) of the circuit for output voltage is evaluated as 23 ppm/ .

In R_L loading of 10-Ω, Fig. 8 shows the maximum output reference voltage 448.411 μV and minimum reference voltage 447.276 μV. The TC also keeps 23 ppm/ . Figs. 9-13 show the TC variations for loading resistances in 100 Ω, 1 kΩ, 10 kΩ, 20 kΩ and 30 kΩ respectively. In Fig. 9, the maximum reference voltage is 4.484 mV and the minimum reference voltage is 4.473 mV. In Fig. 10, the maximum reference voltage is 44.827 mV and the minimum reference voltage is 44.714 mV. In Fig. 11, the maximum reference voltage is 446.957 mV and the minimum reference voltage is 445.850 mV. In Fig. 12, the maximum reference voltage is 892.618 mV and the minimum reference voltage is 890.172 mV. In Fig. 13, the maximum reference voltage is 1.33V and the minimum reference voltage is 1.3266V. Obviously, Figs.7-13 shows the TC of the voltage reference almost keeps on 23 ppm/ in range of loading resistance of 1 Ω to 30 kΩ. Finally, according to these data, Fig. 14 shows the corresponding TC value.

The layout of proposed circuit is shown in the left part of Fig. 15, and the chip area is 534.55 × 694.85 um^2. After layout phase, the parasitic effects are also extracted. The post-layout simulation in loading R_L of 1-Ω is shown in Fig. 16. Since the effects of parasitic resistance and capacitance, the TC of the reference voltage is raised from 23 to 26 ppm/ . The chip fabrication is achieved already. The micro-photo of the chip is shown in right part of Fig. 15. When under temperature 25 ℃ and loading R_L 27 kΩ, the output of the voltage reference is 1.07 V (39.629 uA × 27 k) for 3-V supply voltage and 1.12 V (41.48 uA × 27 k) for 5-V supply voltage. The digital oscilloscope (TBS1052B-EDU) by Tektronix is used to measure the experimental chip for output voltage. Figures 17 (a) and (b) show the measured results for 3-V and 5-V supply voltage respectively. In addition, when temperature on the surface of the chip is risen to 100 ℃, the variation of output voltage is not revealed by using the digital oscilloscope due to 3% measurement accuracy of this instrument.
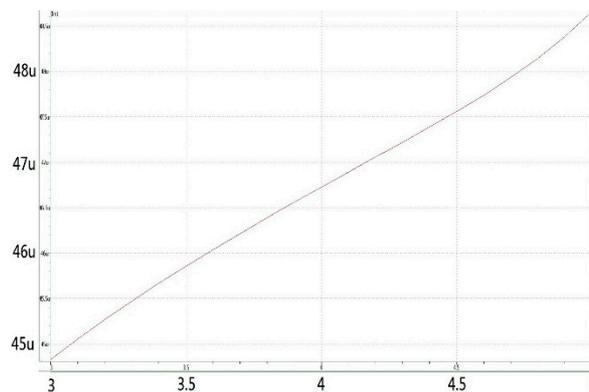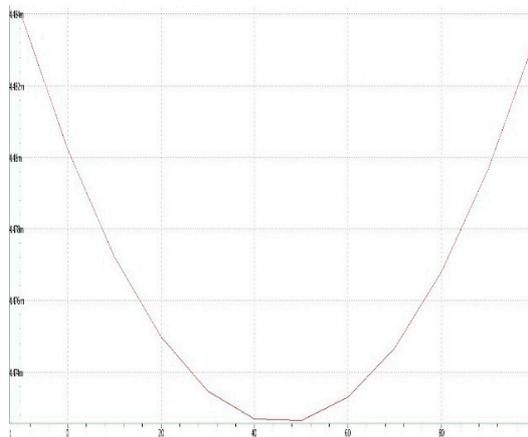

Figure 6. The line regulation of proposed circuit when supply voltage varied from 3 to 5 V.
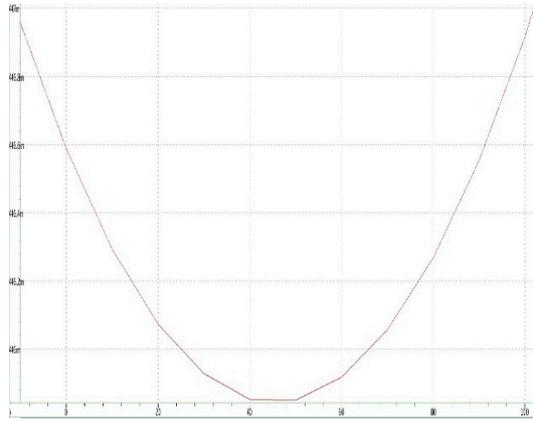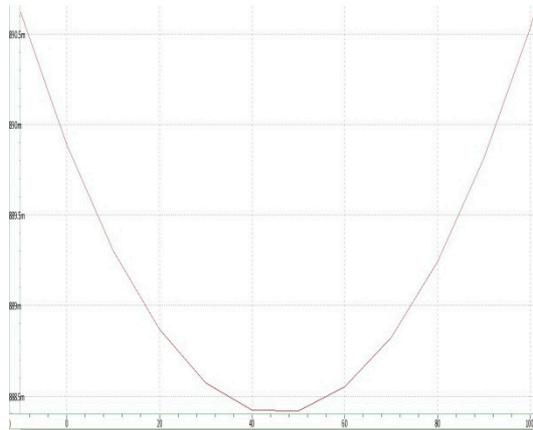

Figure 7. The temperature coefficient of output current in loading resistance of 1 Ω.
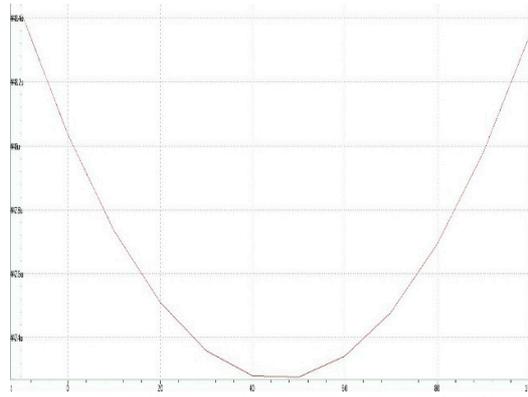
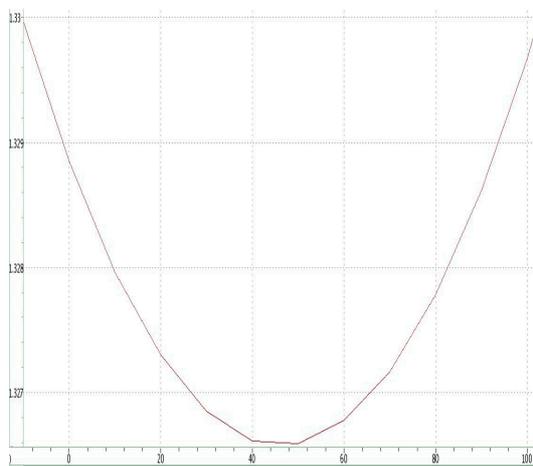**Figure 8.** The temperature coefficient of output current in loading resistance of 10 Ω.

Figure 9. The temperature coefficient of output current in loading resistance of 100 Ω.

Figure 10. The temperature coefficient of output current in loading resistance of 1 kΩ.

Figure 11. The temperature coefficient of output current in loading resistance of 10 kΩ.

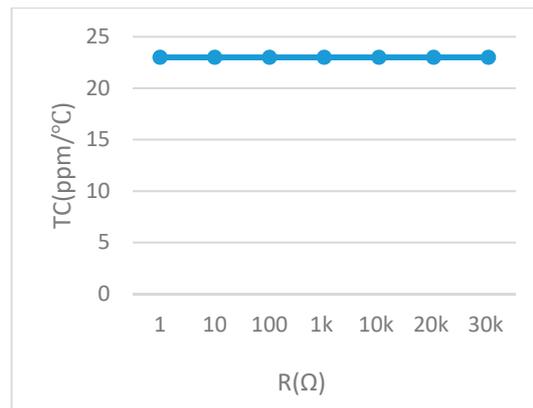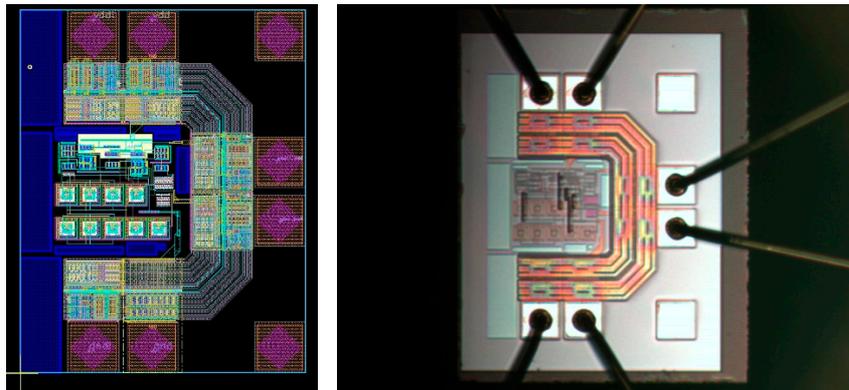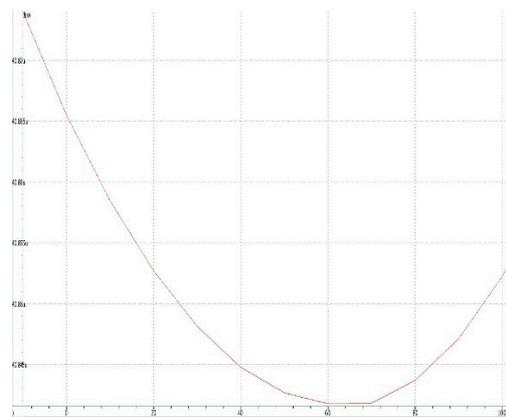**Figure 12**. The temperature coefficient of output current in loading resistance of 20 kΩ.

Figure 13. The temperature coefficient of output current in loading resistance of 30 kΩ.

Figure 14. The corresponding TC value under various resistance loadings.

Figure 15. The layout diagram (left) and micro photo (right) of the resembled bandgap reference circuit

Figure 16. The temperature coefficient of output current in loading resistance of 1 Ω (by post-layout simulation).
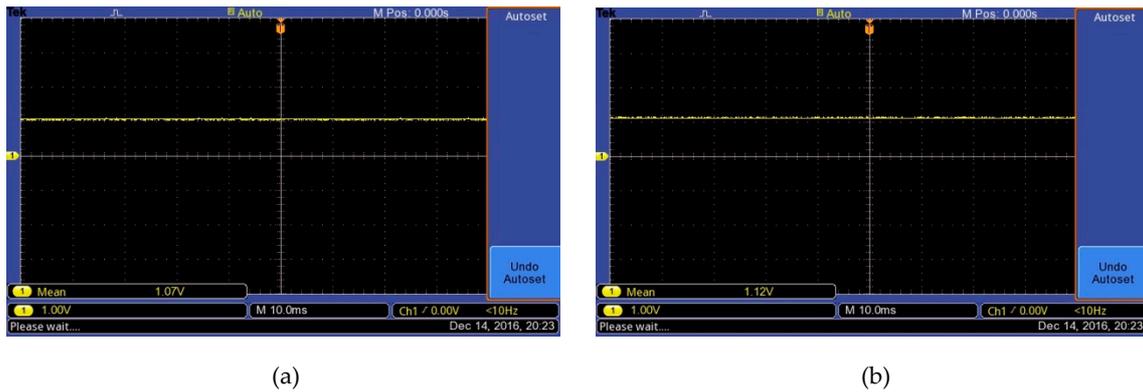
(a)   (b)

Figure 17. The output voltage of the experimental chip for (a) 3-V and (b) 5-V supply voltage respectively.

The characteristics of the proposed circuit summarize and list in Table 1. The characteristics are also compared with reference [1]. The proposed has advantages of low complexity, less chip area, and wide range of output voltage.

Table 1. The characteristics summary and comparison

Characteristics	[1]	This work
Process	CMOS 0.35 μm	CMOS 0.35 μm
Operational Amplifier Required	Need Two OPAs	None
Power supply (V)	0.5	3
Temperature coefficient (ppm/)	13	26 (simulation)
Temperature range ( )	-25 - 125	-10 - 100
No. of Transistor	23	11 MOS + 2 BJT
Circuit Complexity	High	Low

4. Conclusions

In contrast to conventional bandgap reference, the ratio of R_L and R_1 is almost constant value to fully eliminate the temperature effect. The output level of the bandgap reference in conventional design is always constant. In this work, we try to generate the current with positive temperature coefficient and a counterpart current with negative temperature coefficient. The two current then are summed at output terminal to cancel the temperature effect of each other. In addition, the output level will be adjustable by altered the loading resistance. In this design, the complicated design for OPAs can be neglected to reduce the overall circuit complexity. By simulation, the TC was inspected for the loading of 1 Ω, 10 Ω, 100 Ω, 1 kΩ, 10 kΩ, 20 kΩ, and 30 kΩ. The TC will be kept around 23 ppm/ when temperature is varied from −10 to 100 . Although the TC is not superior to other designs have been published in open literature which range of 10-15 ppm/ , the chip area and chip design effort are both great reduced.

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